

# Crosstalk bandwidth and stability analysis in graphene nanoribbon interconnects



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## ABSTRACT

Based on transmission line modeling (TLM), and using the Nichols chart, we present a bandwidth and stability analysis, together with step time responses, for coupled multilayer graphene nanoribbon (MLG NR) interconnects that is inquired for the first time. In this analysis, the dependence of the degree of crosstalk relative stability for coupled MLG NR interconnects comprising of both capacitive and mutual-inductive couplings between adjacent MLG NRs has been acquired. The obtained results show that with increasing the length or decreasing the width of the MLG NRs, the stability in near-end output increases. While, any increase in the length or width of MLG NRs, decrease the stability of far-end output. Also, by increasing capacitive coupling or decreasing inductive coupling, the near-end output becomes more stable, and the far-end output becomes less stable. Moreover, any increase in the length or capacitive coupling, decreases the bandwidth, whereas any increase in the width or inductive coupling, increases the bandwidth. Finally, transient simulations with Advanced Design System (ADS) show that the model has an excellent accuracy.

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## 1. Background

As process technology continues to scale downward from micrometer-to-nanometer, the traditional materials (such as Al and Cu) based interconnects have become serious concerns due to the increased resistivity, susceptibility to electromigration [1,2], short mean free path [3], and strait maximum current density [4]. In the past several years, graphene has attracted much attention due to its superior properties, such as extreme high current carrying capability [2,4,5], long mean free path (i.e.,  $\sim 1 \mu\text{m}$  at room temperature [3,4]), ballistic transport [6,7], high intrinsic mobility [7–9], high thermal/electrical conductivity [9], and straightforward fabrication processes [2,6,10]. The monolayer GNRs electrical intrinsic resistance is too large to be applicable. In order to surmount this problem, MLG NRs which have lesser resistance, must be used in interconnect applications [11]. Generally, VLSI circuits consist of several same interconnects that are adjacent to one another. Parasitic elements, includes mutual inductive and capacitive effect generated between adjacent interconnects, makes crosstalk phenomenon. Crosstalk is an extra serious matter in VLSI

circuits due to adverse effects such as, overshoot/undershoot [12], delay [13,14], glitch [13]. Therefore, crosstalk makes serious problem for reliable operation of an interconnect application.

A closed-form expressions for worst-case time delay due to the crosstalk of coupled interconnect in terms of distributed RC line and considering the parasitic coupling capacitive effect derived in Ref. [15]. The closed-form expressions in previous work, extended by [16] in terms of distributed RLC line and considering the both parasitic coupling effects.

In [1] crosstalk analysis is presented for GNRs based interconnects and compared with copper and multiwall carbon nanotube (MWCNT) by calculating Crosstalk induced noise and overshoot/undershoot. In [17] signal integrity analysis for single layer GNR and MLG NR interconnects are carried out based on the coupled interconnect with parasitic coupling capacitances. A time and frequency sphere model is presented in [18,19] for analysis of crosstalk effects in CNTs based interconnects.

Crosstalk effect of two single-wall Carbon Nanotubes (SWCNTs) are considered in [20], and also crosstalk induced noise has been modeled by statistical alteration of interconnect parameters due to process alteration. An analytical crosstalk model of the peak noise for coupled interconnects with a shield between the lines is presented in [21]. For reduction crosstalk effects some approach such as shield insertion between coupled interconnects, gate

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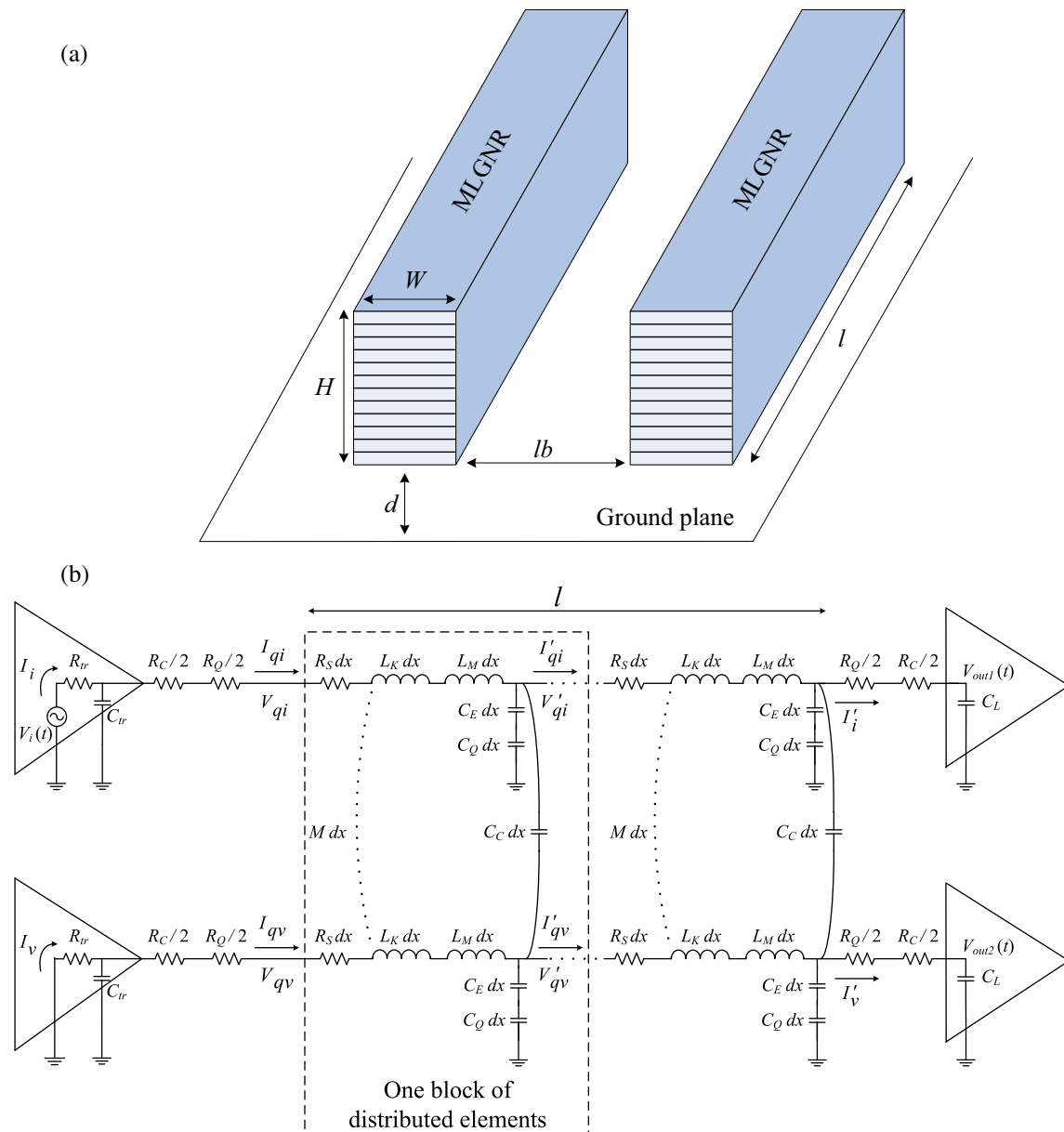
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sizing, low dielectric constant, and double-layered dielectric interconnects are presented in [21–24] respectively.

In addition to the works mentioned, several researches have undergone to inquire the applicability of GNRs and CNTs as VLSI interconnects. A number of studies on GNR-based interconnects for, signal transmission, relative stability, low swing signaling, and time domain analysis have been found in [6,11,25,26]. The works in [27–30] have inquired the performance evaluation of CNTs based interconnects.

In some applications, in addition to the system absolute stability, its relative stability is also an important parameter [31]. In order to find the relative intensity of the systems, the step response is a useful benchmark, while overshoot is smaller, the system is more stable. A Nichols chart displays the open-loop magnitude (in dB) plotted against the open-loop phase (in degrees) of the system response [32]. The critical point is, intersect of 0-dB axis and  $-180^\circ$  axis. The phase crossover frequency is where the locus intersects the  $-180^\circ$  axis, and the gain crossover frequency is

where the locus intersects the 0-dB axis. Gain crossover frequency is approximately equal to the bandwidth of the system, so a larger gain crossover frequency corresponds to faster response, but also leads to smaller phase margins [32]. Also, maximum magnitude peak of Nichols chart is related to the damping ratio and overshoot. In a Nichols chart, phase margin (PM) is the horizontal distance (measured in degrees) between the gain crossover point and the critical point (0-dB,  $-180^\circ$ ), and gain margin (GM) is the distance (in decibels) between the phase crossover point and the critical point. The system becomes more stable if the GM and PM increase [32]. In fact, in bandwidth and stability analysis with evaluating open loop system, the behavior of the closed-loop system is predicted. On the other hand, a chip interconnects are used in both open and closed loop systems. Hence, any change in stability and bandwidth of an open loop system such as interconnects leads to change in stability and bandwidth of closed-loop systems on the chip [33]. In this paper, we present a matrix formulations for equivalent circuit model of coupled MLGNR interconnects, based



**Fig. 1.** (a) Geometry of double coupled MLGNR interconnects on a ground plane and (b) its TLM circuit model. Dash frame represents one of the NB distributed blocks of length  $dx = l/NB$ .

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