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Interplay of plasma etch, strip and wet clean in patterning La_2O_3/HfO_2-containing high-κ/metal gate stacks

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ABSTRACT

The removal process of the La_2O_3/HfO_2 dielectric and of the residues after metal gate etch are discussed. The challenges are presented and related to the specific physico-chemical properties of La-containing compounds. Solutions based on optimization of plasma etch, strip and wet clean are demonstrated for both an integrated and delayed etch–clean process. Both processes meet the stringent requirements of complete removal of the high-κ layers and metal-containing sidewall residues without inducing silicon recess or undercut.

1. Introduction

The implementation of advanced high-κ and metal gate materials in front-end-of-line (FEOL) processing for the 45 nm CMOS generation induces many challenges with respect to dry etch and wet clean. Conventional poly-silicon (poly-Si) gates on silicon dioxide (SiO_2) dielectric layers are replaced by metal gates such as TiN or TaN and high-κ dielectric materials such as hafnium oxide (HfO_2) [1]. Further optimization of the device performance is achieved by introducing cap layers to modulate the work function and to improve reliability [2–4]. Candidate capping materials for NMOS transistors include La_2O_3, MgO_2 and BaO_2; candidates for PMOS transistors include Al_2O_3 and TiO_2.

The process development of such complex gate stacks requires systematic investigation of different etching, stripping and cleaning conditions for each stack. A major challenge is the complete removal of the high-κ and capping layers without inducing silicon recess or undercut [5]. The low volatility of the high-κ-containing compounds hinders dry removal, while crystallinity of the layers often prevents wet removal. Furthermore, cleaning metal-containing post-etch residues from the gate sidewalls without attacking the metal is a stringent requisite that complicates the process.

A combined dry–wet process is generally applied for high-κ removal [5]. In the dry process, BCl_3 plasmas are commonly used as these chlorinate the metal oxide and decrease the silicon etch rate for the poly-Si gate and Si substrate through formation of a boron-containing passivating film. The key challenge is the low volatility of the etch products formed during high-κ etch. Typical wet etch chemistries for Hf-based materials are diluted hydrofluoric acid (HF)-based solutions, where hydrochloric acid (HCl) is added to improve the selectivity towards SiO_2 [6]. In contrast, La_2O_3 is soluble in HCl, but forms insoluble LaF_3 in HF solutions and as such forms particles [7–9]. Clearly the removal of La_2O_3/HfO_2 stacks is complicated by this apparent chemistry incompatibility.

In this article, we investigate the interplay between dry etch, strip and wet clean/etch of La_2O_3/HfO_2-containing gate stacks. Conditions for the dry and wet process steps for complete high-κ removal with good residue control are explored. Moreover, the effect of delay time between dry and wet cleaning steps has been evaluated.

2. Experimental

This study was performed on a Lam Research 2300® cluster tool with Kiyo® conductor etch chambers, a Microwave Stripper chamber and a Serene® single-wafer wet clean process module, utilizing C3™ (Confined Chemical Cleaning) technology.

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The gate stack comprised of the following layers (from bottom to top): $SiO_2/HfO_2/La_2O_3$/physical vapor deposited (PVD) TaN/PVD TiN/amorphous Si (a-Si)/amorphous carbon (a-C)/SiOC/193 nm-photoresist. HfO_2 and La_2O_3 layers were deposited with an atomic layer deposition (ALD) process and were in the thickness range of 0.5–1.5 nm. The TiN and TaN layers were 3 and 7 nm thick, respectively. For high-κ removal screening tests, blanket HfO_2/La_2O_3 layers were deposited, followed by an annealing step with a similar thermal budget as for the patterned wafers.

The patterned wafers were etched using a $CH_2F_2/SF_6/N_2$-based chemistry for the silicon main etch, followed by HBr/O_2 plasma during soft landing and over-etch. The metals were etched using HBr/Cl_2; the a-C mask was stripped with O_2/Cl_2. Gate profile optimization was ongoing at the time of this study. For the wet clean processes using an HF/HCl mixture, exposure times were on the order of 2–5 s.

Blanket wafers were analyzed with Rutherford Back-Scattering (RBS) to measure the coverage of the remaining Hf and La, or the number of atoms per unit area, using 2 MeV He scattering. The removal of the high-κ layers was also studied with total reflection X-ray fluorescence (TXRF) on a Rigaku TXRF-300 system. The measurement was performed on individual points, with a short integration time of 5 s. This method allows for wafer mapping, although with a detection limit a factor of 10 worse than direct TXRF.

Scanning electron microscope (SEM) photographs have been taken in top-down orientation on an eCD SEM from KLA-Tencor and in tilted mode on an Expida 1285 SEM from FEI. Transmission electron microscope (TEM), scanning transmission electron microscope (STEM), energy dispersive X-ray spectroscopy (EDX), and electron energy loss spectroscopy (EELS) analyses were performed with an FEI Tecnai (F30) FEG transmission microscope operating at 300 kV. The tool is equipped with a post-column Gatan Imaging Filter (Tridiem-GIF) an energy dispersive X-ray spectrometer (EDAX) and an STEM unit. The TEM specimens were oriented with the ⟨1 1 0⟩ crystallographic direction of the silicon substrate parallel to the electron beam.

The relative humidity of a FOUP was varied from ambient conditions (~40% relative humidity) to dry conditions by the addition of $CaSO_4$ desiccant bags. The relative humidity level was measured over time and the value stabilized within 1 h to <15%. For the storage in N_2, a single wafer was placed in a cupboard purged with 0.5 bar N_2. The relative humidity in the N_2 cabinet was <20%.

3. Results and discussion

3.1. Characterization of gate structures after plasma etch

In the first phase of this study, TEM–EDX was used to characterize the location, size and composition of the residues formed after the a-Si etch, metal gate etch and a-C mask strip. The dry etch recipe was not yet optimized for the gate profile and a notch in the lower part of the Si layer and a foot in the metal gate layer were observed. A non-continuous layer of TaO_x-containing residues was detected on the top and on the sidewalls of the feature (Fig. 1). Hafnium and oxygen were present in the active area of the structure. Lanthanum was not detected; this can be explained by the fact that the capping layer is very thin (below detection limits) and is most probably intermixed with the HfO_2. Taking the TEM analysis results into consideration, two major targets were put forward: (1) the cleaning of metal-containing post-etch residues from the gate sidewalls without attacking the gate stack and (2) the selective and complete removal of high-κ and capping layers.

3.2. High-κ removal study on blanket wafers

The removal of the high-κ layers on blanket wafers using a BCl_3 dry-only approach was studied by RBS (Fig. 2). This BCl_3 chemistry is often applied in the dry etch as it chemically reduces and chlo-

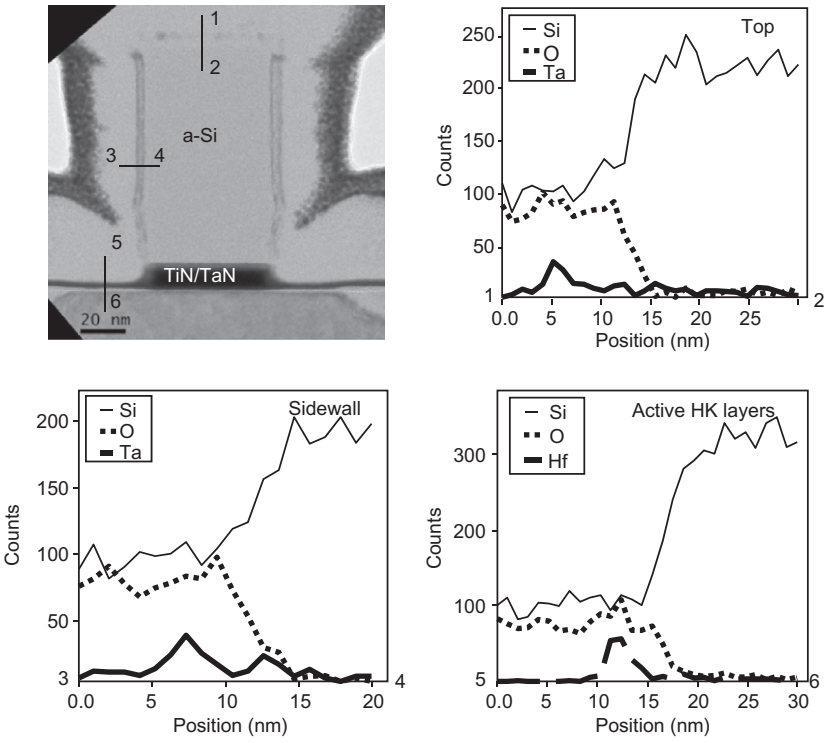

Fig. 1. TEM–EDX line scans of silicon/metal gate/high-κ feature after metal gate etch.