Microelectronics Reliability 55 (2015) 789–794

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

# Potentiality of trap charge effects and SiON induced interface defects in a-$Si_3N_4$/SiON based MIS structure for resistive NVM device

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ARTICLE INFO

*Article history:*
Received 25 February 2014
Received in revised form 6 January 2015
Accepted 6 February 2015
Available online 26 February 2015

*Keywords:*
PECVD
Amorphous silicon nitride
Resistive switching
Trap charge
Memory window
Non-volatile memory

ABSTRACT

Potential application of amorphous silicon nitride (a-$Si_3N_4$)/silicon oxy-nitride (SiON) film has been demonstrated as resistive non-volatile memory (NVM) device by studying the Al/$Si_3N_4$/SiON/p-Si metal–insulator–semiconductor (MIS) structure. The existence of several deep trap states was revealed by the photoluminescence characterizations. The bipolar resistive switching operation of this device was investigated by current–voltage measurements whereas the trap charge effect was studied in detail by hysteresis behavior of frequency dependent capacitance–voltage characteristics. A memory window of 4.6 V was found with the interface trap density being $6.4 \times 10^{11}$ $cm^{-2}$ $eV^{-1}$. Excellent charge retention characteristics have been observed for the said MIS structure enabling it to be used as a reliable non-volatile resistive memory device.



## 1. Introduction

Silicon nitride ($Si_3N_4$) plays an important role in electronic and optoelectronic devices due to its high resistivity, mechanical strength, chemical stability and high dielectric constant [1]. Furthermore, $Si_3N_4$ thin film has a great importance in metal–insulator–semiconductor field effect transistors (MISFET) and thin film transistors (TFT) as it can be used as gate dielectric [2]. The potential application of $Si_3N_4$ as an active switching element for each pixel in a display [3] and as active charge-storage insulator for non-volatile memory devices [4,5] has also been widely investigated in recent years.

The memory effects of the metal–insulator–semiconductor (MIS) structures have been related with the charge capture in memory traps of the $Si_3N_4$ film. The memory traps referred to as electron or hole localized states (within the band gap of the $Si_3N_4$ film) are generally associated with impurities or defects in the insulator [6]. Electrical conductivity of a-$Si_3N_4$ as a dielectric is also dominated by trapped charge with intermediate energy levels around the Fermi level [7]. Notably, the imperfections or defects within the same material as well as at the interface between different materials are held responsible for charge trapping. By using electrical techniques such as capacitive and conductive methods, bulk and interface traps of nitride based MIS device can be characterized [8]. The values of the density of interface traps, $D_{it}$, are indicated by defect levels in the silicon-nitride band gap and are reported to be within the range of $1 \times 10^{11}$–$5 \times 10^{12}$ $cm^{-2}$ $eV^{-1}$ [9].

Moreover, during the formation of $Si_3N_4$, SiON may form at the interface of Si and $Si_3N_4$ which can induce interface defects [10]. All the defects in oxy-nitride film such as paramagnetic defects, diamagnetic defects, dicoordinated Si center and neutral defects are responsible for creating dielectric traps [11]. So, SiON may enhance the charge storage effect coupled with the presence of $Si_3N_4$. However, till now the potential performance aspects of $Si_3N_4$ with SiON as NVM device as well as a switch have not been fully explored. In the present study, efforts have been made to study the deep trap levels [12] as the most important factors for such non-volatile-charge storage devices. Electrical properties such as current–voltage ($I$–$V$) and capacitance–voltage ($C$–$V$) characteristics were emphasized to investigate the capacitance ($C$), conductance ($G$), ideality factor ($\eta$) and flat-band voltage ($V_{FB}$) of the NVM device. In addition, the deep levels were also studied by photoluminescence spectroscopy and correlated with the as-found traps from electrical characteristics.

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http://dx.doi.org/10.1016/j.microrel.2015.02.013
0026-2714/

## 2. Experimental procedure

Various techniques such as chemical vapor deposition (CVD) [13], low-temperature based plasma-enhanced CVD [14], electron-cyclotron resonance CVD [15], and sputtering techniques [16] have been reported for the deposition of $Si_3N_4$ thin films. Among them, PECVD is generally chosen not only to reduce thermal budget, but also to achieve more flexible film [17,18]. Additionally, due to generation of high frequency plasma in PECVD system, the grown $Si_3N_4$ film shows less dielectric charging and better electrical characteristics as required for microelectronics applications [19]. Further advantages of PECVD technology are high deposition rates, high precursor utilization, and high quality dense films. In PECVD technique large area deposition occurs at an instance [20].

For the present investigation, silicon nitride ($Si_3N_4$) was deposited on p-Si (100) substrates by means of PECVD (OXFORD make) system. Prior to growth, the sample was degreased by boiling with trichloroethylene, acetone and methanol successively for 10 min. Next, the native oxides of the samples were etched through a dipping in 2% HF solution followed by repeated rinsing in DI water. Then, the samples were immediately loaded to the growth chamber to avoid re-oxidation. Silane ($SiH_4$) and nitrogen ($N_2$) were used as the precursors for Si and N, respectively. All the relevant growth parameters are given in Table 1.

For the contacts, aluminium (Al) was deposited by thermal evaporation followed by an annealing at 300 °C in both the surfaces of the sample. The electrical measurements, such as current–voltage (*I–V*) and capacitance–voltage (*C–V*) were conducted using Keithley 2400 and 4200 semiconductor characterization systems (SCS), respectively. Also, room temperature photoluminescence spectra of the sample were acquired by Accent Nanometrics RPM 2000 to get an insight into defect related states in the as-grown film.

## 3. Results and discussions

A schematic cross-sectional view of the fabricated Al/$Si_3N_4$/SiON/p-Si MIS device is shown in Fig. 1a. The thickness of the $Si_3N_4$ film was measured to be about 100 nm by ellipsometry. The interfacial regions of the structure were further scrutinized by cross-sectional transmission electron microscopy (TEM) imaging as shown in Fig. 1b. The presence of an silicon oxy-nitride (SiON) of 4 nm thickness in between the Si and $Si_3N_4$ was revealed from the analysis of the bright field (BF) images, and the thickness of $Si_3N_4$ was reconfirmed. This SiON film aided to increase charge trapping effect due to the formation of nitrogen induced interface defects.

In this aspect, we have studied the photoluminescence (PL) spectroscopy of the deposited a-$Si_3N_4$ to find out the trapped levels. Earlier, Anutgan et al. [21] had reported a general consequence of silicon-rich-a-$Si_3N_4$ (SRSN) deposition by PECVD system. This SRSN system exhibits a very notable photoluminescence which reveals the formation of interface states acting as a recombination centers [22]. These interfacial states reportedly originated from Si–Si, Si–N bonds, and from the structural and compositional disorders at the interface [23]. Fig. 2 shows the photoluminescence (PL) spectrum of the present amorphous silicon nitride-silicon structure. The PL spectrum exhibits a broad peak around 2.2 eV (553.8 nm). Gaussian fitting of the entire luminescence spectra [24] gives the information about emission bands (2.15 eV, 2.19 eV, 2.23 eV, 2.27 eV and 2.30 eV) of $Si_3N_4$ which are caused by different excitonic transitions between the defect levels and corresponding band as well as between the defect levels themselves [25,26]. In a previous study it was observed that all the emission bands in between 2 and 3.2 eV correspond to trap levels (defect levels) in $Si_3N_4$ film [25–27]. As it is confirmed from the various experiments that follow, these same defect levels consequently give rise to memory effect by charge accumulation in nitride film as a result of transitions of electrons and holes into these traps [28].

**Table 1**
The optimized parameters utilized for $Si_3N_4$ film deposition.

| Temperature | Pressure | Flow rates (sccm) | | RF frequency |
|---|---|---|---|---|
| | | Silane | Nitrogen | |
| 300 °C | 200 mTorr | 2 | 940 | 13.56 MHz |

Fig. 3 shows the cyclic current–voltage characteristics of the MIS device. The curves show a bipolar resistive switching behavior in the sequence of swept voltages from 0 V to +10 V and +10 V to 0 V in forward bias, and also from 0 V to −10 V and −10 V to 0 V in reverse bias. Initially, there occurs a forming process due to sudden increase of current level (from 0 to +10 V) when transition takes place from high resistance state (OFF state) to low resistance state (ON state) [29]. From the *I–V* characteristics it has been found that in between the sweeping mode (0–10 V), two states, viz., OFF and ON state have been occurred. Initially, while the forward bias was applied the device remains in the OFF state until the threshold voltage ($V_{th} \sim 4.6$ V) is reached. At $V = V_{th}$, the device current increases almost $10^4$ times than that of the OFF state, and consequently ON state is achieved. Such ON state continues with the further increase of the applied bias voltage. By sweeping the voltage from +10 V to 0 V, a second jump from a low resistance state (ON state) to the high resistance state (OFF state) is observed at 1.2 V. Notably, the current did not retreat following its previous transition from OFF state to ON state. A similar resistive switching behavior has been found in the reverse bias also.

Here it should be mentioned that for sufficiently thick dielectric layers on silicon, the charge conduction mechanism is governed by bulk traps [30]. Previously, the conduction mechanism of the $Si_3N_4$ insulating film has been explained through the Frenkel–Poole mechanism [31,32] in which there occurs an emission of electrons from traps into the conduction band [33]. Theoretically, this conduction mechanism is expressed by the relation between *J* and *E* [8]

$$J = C \times E \exp \frac{-q\left[\varnothing_t - \sqrt{\frac{qE}{\pi\varepsilon_0\varepsilon_r}}\right]}{kT} \quad (1)$$

where *J* is the current density (A/cm$^2$), *C* is the preexponential factor, *E* is the electric field (V/cm), *q* is the electric charge ($1.602 \times 10^{-19}$ C), $\varnothing_t$ is the barrier height of electrons for emission from trap state (V), $\varepsilon_0$ is the permittivity of vacuum ($8.854 \times 10^{-14}$ F/cm), $\varepsilon_r$ is the relative dielectric constant, *k* is Boltzmann's constant ($1.38066 \times 10^{-23}$ J/K), and *T* is the absolute temperature (K). In Fig. 4a, the log(*J*/*E*) vs $E^{1/2}$ characteristics is observed to yield a linear fit in the high conduction region for our specimen. Though the plot suggests that the current density exhibits field dependence according to the said law, but the value of high frequency relative dielectric constant extracted from the curve is orders more than theoretically predicted value [34]. Additionally, the nature of conduction was also scrutinized from the plot of log(*J*/*E*) vs *E* as shown in Fig. 4b. A linear fit for this curve is again obtained, inferring that the current–voltage characteristics is more likely to follow Poole's law ($\sigma = \sigma_0 e^{\alpha E}$, where $\sigma$ is the conductivity), a conduction mechanism more suitable for solids with ionized defects in such high density that their coulombic potentials can overlap one another [35]. Alternately, in recent studies, [34,36] multi-phonon trap ionization has been proposed as a probable transport mechanism in $Si_3N_4$ which may describe the present case with emission-and-capture from the multiple discrete trap levels as