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Effect of electric field polarity on inter-poly dielectric during cell operation for the retention characteristics

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ABSTRACT

Retention characteristic represents a capability to maintain the storage data and it is related with the reliability of memory device. The retention characteristic is degraded by the leakage of charges from a floating gate to a control gate, and thus the leakage current at low and moderate electric field of inter-poly dielectric (IPD) is one of the important characteristic for floating gate type flash memories. In addition, it is necessary to investigate the effects of the electric field polarity on the electric characteristics of IPD because the electric field polarity is changed as the cell operations such as the programming and erasing. Therefore, in this paper, the variation of the leakage current of IPD at moderate electric field region is measured with varying the previously applied electric field polarity. Based on the result, the effect of sequential change of an applied electric field polarity on the electrical characteristics is analyzed.

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1. Introduction

A non-volatile NAND flash memory has been scaled down to improve its performance in terms of the speed, density, and power consumption. The multi-level cell (MLC), which has several program states such as double and tri-program levels, has been also used for high programmable bits [1]. The threshold voltages (V_{th}) of various program levels are distributed sequentially in the MLC and the margin of the V_{th} is reduced compared to that of single-level cell (SLC). In MLC, even a small distortion of the V_{th} distribution can induce a data error due to an incorrect decision of the cell bits [1,2]. Especially, the tail bits phenomena of the V_{th} distribution can cause the serious problem. The distortion of the V_{th} distribution can be induced by the leak of charges in the floating gate (FG) which is related to the leakage currents of the inter-poly dielectric (IPD) and tunneling oxide (T_{ox}).

To improve the data retention, the relationships between the data retention and electrical characteristics of IPD and T_{ox} with various stress conditions have been previously investigated [3–7]. In addition, the degradation of IPD with various oxide thicknesses was investigated using the injected charge to breakdown and time to breakdown [3–5]. The V_{th} distribution shift was also demonstrated with respect to the bake time [6]. Moreover, retention modeling with silicon oxide–silicon nitride–silicon oxide (ONO) scaling was investigated using statistical analysis [7].

However, the effect of previous cell operations, such as a program and an erase, on the leakage current at low and moderate electric field regions has not been demonstrated. It is important to analyze the electrical characteristic of IPD with varying the previous electric field polarity, because the electrical properties of IPD at low and moderate electric field regions are related to the data retention and it is affected by the previous applied electric field. The electric field polarities were changed for cell operations such as programming and erasing. In this paper, the variations of the electrical characteristics of IPD at moderate electric field varying with the previously applied electric field polarity were investigated.

2. Experiments and measurements

The ONO test structure was fabricated on 12-in. wafers using the 2x NAND flash process by SK Hynix Semiconductor Inc. The test structure of the IPD was constructed with the ONO stack sandwiched with two heavily doped poly-Si layers, which are the FG and the control gate (CG), as schematically shown in Fig. 1. The silicon oxide (bottom), silicon nitride, and silicon oxide (top), called as ONO stack, were sequentially grown by LPCVD [8,9].

To analyze the leakage current variation with a recursive electric field, the current–voltage (I–V) and capacitance–voltage (C–V) characteristics were measured using an Agilent 4156C parame-

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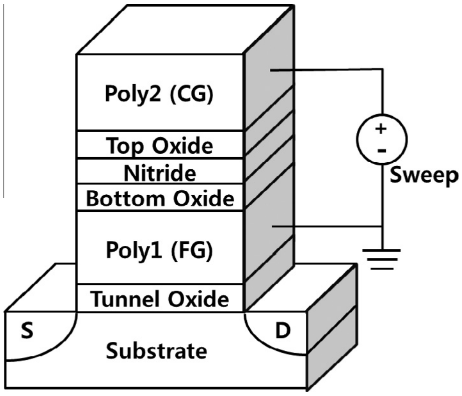

Fig. 1. Schematics of the test structure and bias condition.

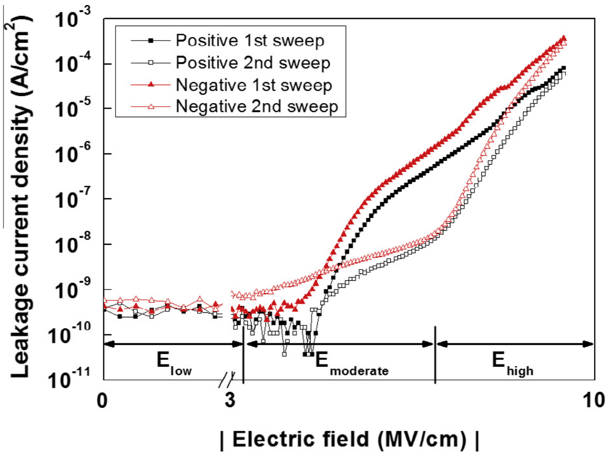

Fig. 2. Leakage current densities of the initial and second sweeps of the ONO stack for positive and negative polarities.

ter analyzer and an Agilent 4980 LCR meter at 10 kHz, respectively. The leakage current density–electric field (*J–E*) characteristics were then calculated from the *I–V* curves, which were the applied bias divided by the equivalent oxide thickness (EOT) of the ONO stack. To apply the external voltage to IPD, the external bias and ground were applied to CG and FG, respectively, as shown in Fig. 1. The negative bias was swept from 0 to −9 MV/cm, which is similar with the cell erasing operation. Moreover, the opposite polarity bias compared with the previously applied bias polarity was swept from 0 to 9 MV/cm to investigate the effect of the difference for sequentially applied electric field polarities. The capacitance was measured from −5 V to 5 V after *I–V* sweep to verify the relationship between the leakage current and trapped charges when the external voltage is applied. Here, since the range of the *C–V* measurement is small compared with the *I–V* measurement, it does not affect the trapped charges.

3. Results and discussion

Since the electric field polarities during the cell programming and erasing operations were opposites, the leakage currents of the ONO stack were measured for the positive and negative polarities. As shown in Fig. 2, the tendency of the leakage current was similar for both polarities but the leakage current of the negative sweep was higher than that of the positive sweep. The difference in the leakage currents was due to the asymmetry of the ONO structure, such as the thicknesses of the top and bottom oxides and the doping concentrations of FG and CG [10]. However, the leakage current at low electric field was too low to be measured precisely due to the measurement resolution, so the variations of the leakage current were analyzed using the leakage current at moderate electric field.

The electrical characteristics for the recursive negative sweep were illustrated in Fig. 3. The *J–E* curve was shifted in the positive direction as the number of sweeps was increased because of the charge trapping [11–13]. The changes in the *J–E* and *C–V* curves between the initial sweep and the 2nd sweep were significant. The changes in the electrical characteristics after the 2nd sweep were small but continuous. In other words, the charges were trapped consistently in the ONO stack when the external electric field was applied. It indicates that the charge trapping was caused during the cell operation due to the applied electric field induced by the coupling ratio between the CG and FG.

To investigate the effect of sequentially applied electric field polarities on the retention characteristic, the positive external bias, which was the same electric field polarity as the programming operation, was applied after applying the negative sweep which was the same electric field polarity as the erasing operation. The variations in the leakage currents for the negative and positive sweeps were shown in Fig. 4(a). Here, the sweeps A, B, and C were measured sequentially. The leakage current for sweep B, which is applied positive polarity bias, was measured immediately after sweep A, which is applied the negative polarity bias. The leakage current of sweep C was then re-measured with the same sweep polarity of sweep B. It was observed that the leakage current at moderate electric field increases from sweep A to sweep B but

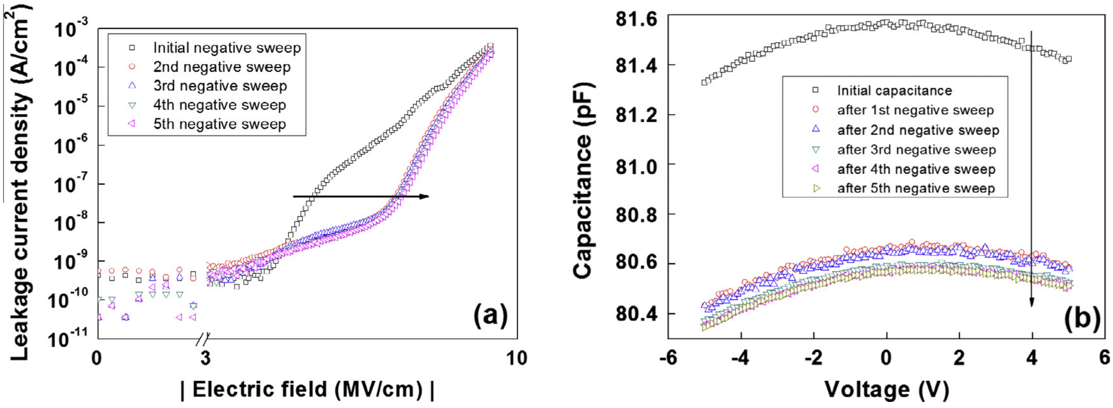

Fig. 3. The electrical characteristics of ONO stack for recursive negative sweep applied to the CG: (a) *J–E* curves with five recursive sweeps and (b) *C–V* curves.

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