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Thermal resistance of side by side multi-chip package: Thermal mode analysis

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ABSTRACT

The thermal mode analysis is used in this paper to optimize the thermal management with optimal locations and chip sizes for multi-chip package. The average thermal resistance is defined and analyzed. The spreading thermal resistance can be expanded into Fourier series so that the thermal modes can be established. For the infinite thermal modes, only a few terms are needed to be considered due to the rapid convergence of solution. The optimal locations and chip sizes can then be determined by using the first few modes to reduce the thermal resistance as minimal as possible. The optimal locations have the cosine wave property so that the wave nodes might be the suitable sites. On the other hand, the optimal chip sizes have the cardinal sine property which decays monotonously. For given optimal locations, the optimal chip sizes are determined by certain modes. These special modes can be used to analyze the range of optimal locations and chip sizes.

1. Introduction

The heat generation in semiconductor devices is an important issue since the high power dissipation may lead the device to fail, especially for small size and multi-chip devices. Integration using multi-chip packaging (MCP) is an effective and popular technology option to increase transistor density in one component by integrating two or more dice or other discrete components on a common substrate. For accurate thermal analyses of MCPs, thermal interactions between active components need to be quantified and understood. It is necessary to enhance the thermal management of electronic packages so that the device can exactly work [1]. The enhancing methods commonly adopted are the full simulation to solve the heat equation, then to investigate the trends by changing the interested variables. Generally, the simulation methods are hard to show the trends mathematically. Moreover, the full simulation needs much computational effort. A thermal analysis approach based on the influence coefficient matrix, which represents the thermal resistance from the junction to the case, was successfully developed for predicting cooling capabilities of MCP architectures [2]. Generally, this influence coefficient matrix should be calculated using the data collected with thermal simulations or experiments. The detailed calculation procedures of this matrix have been introduced in the literature [2]. Moreover, some challenges in measuring the thermal resistance of influence coefficient matrix were mentioned [3].

Light emitting diodes (LEDs) are currently the most energy efficient light sources. Multiple-chip packaging becomes common in LEDs packaging community. For such type of packaging, thermal spreading resistance is an important factor to affect the total thermal performance of LEDs. Up to now, the thermal management of high brightness multi-LED packages is still a challenge. Currently, less than one third of the input power of high brightness LEDs is converted into light while the rest is transformed into heat. Improving the thermal management to reduce the LED junction temperature is crucial to enhance the total life time, the efficiency and droop of LEDs. Therefore, modeling the thermal performance of electronic systems to optimize the design is becoming a useful tool to reduce the development time and improve the quality of final product. For instance, Cheng et al. [4] presented an analytical solution to study the whole temperature field and thermal spreading resistances of LED packaging substrate. The feasibility of the analytical method has been proven by the temperature comparison with existing experimental and numerical results of a street lamp. Poelma et al. [5] developed an efficient thermal modeling approach based on finite-element method to design and characterize the thermal performance of an ultra-thin multi-LED package. After verified by the thermal measurements, they concluded that the

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modeling approach can assist in the thermal optimization of future multi-LED package designs.

Component placement problem in high power boards and multi-chip modules (MCMs) has also attracted great attention. Since in many MCMs, thermal management is the most important reliable factor and should be considered as early as possible in the overall packaging process. The best opportunity may be during the chip placement stage, because the temperature distributions are directly related to the result of chip placement. Placement techniques have been developed primarily on the basis of routability. However, due to the increased demand for high quality and long-term reliable performance, techniques are focused to address placement for reliability. For instance, Huang and Fu [6] proposed a thermal force-directed algorithm based on a fuzzy model to manage the thermal placement problem of MCMs. Lee [7] developed a novel thermal force model based on a new force-directed algorithm and heat conduction analogy. This model is appropriate to solve the thermal placement problems of MCMs and hybrid circuits. The proper placement of elements to ensure optimal reliability and desirable levels of temperature coupling for high-power hybrid (HPH) device is proposed by Maly and Piotrowski [8]. Placements for both reliability and wirability considerations are presented for convectively cooled printed circuits boards (PCB) [9]. For other thermal placement methods, it can be referred to the Refs. [10–12]. It should be noted that the thermal resistances defined in these studies are considered as pre-assumed constants.

The package components of electronic devices are usually composed of regular solids so that the Fourier analysis can be applied. Fourier series expansion is a powerful method to analyze the regular system appears in many engineering systems. Wang et al. [13] used the Fourier series expansion to solve the Laplace equation to investigate the effects of metal lead, electric contact resistance, silicon doping concentrations, and microcooler size on the cooling performance of the thermoelectric microcooler. Through optimizing geometry the metal lead effect due to heat generation and heat conduction could be minimized to enhance the cooling performance. Yovanovich [14] and Desai et al. [15] developed the general solution for thermal spreading resistance of one and multiple cylindrical solids, respectively, by using Fourier–Bessel functions expansion. When the cylinder is very long and side cooling is small, the general relationship reduces to the case of an extended surface with end cooling and spreading resistance at the base. They also applied their analytic model to the simulation of a nanotube or nanocylinder connecting a region of the chip to a region of the heat sink. Culham et al. [16] and Geer et al. [17] obtained the analytical solution of the heat conduction in multilayerd rectangular bodies with hyperbolic functions. The general solution through layer by layer analysis is useful to describe the multi-layer substrate in the IC package. They also investigated the application of hot spots in a chip stack with nonuniform heat generation.

Up to now, only few literatures have investigated the problems of MCPs. Muzychka et al. [18] have obtained the Fourier series solution for multiple heat sources. However, the trends of geometry effects were not investigated. In this study, the thermal mode analysis to evaluate the thermal resistance was performed by using the technique of Fourier series expansion. From the features of the thermal modes, the optimal design for the multi-chip package, including the chip location and size optimums, can be achieved.

2. Fourier series expansion

Consider the package having multi-chip (N chips) with locations $\{(X_c^i, Y_c^i)\}_{i=1,\ldots,N}$ and sizes $\{(c^i, d^i)\}_{i=1,\ldots,N}$, as shown in Fig. 1, the governing equation of the system can be expressed by Laplace's equation,

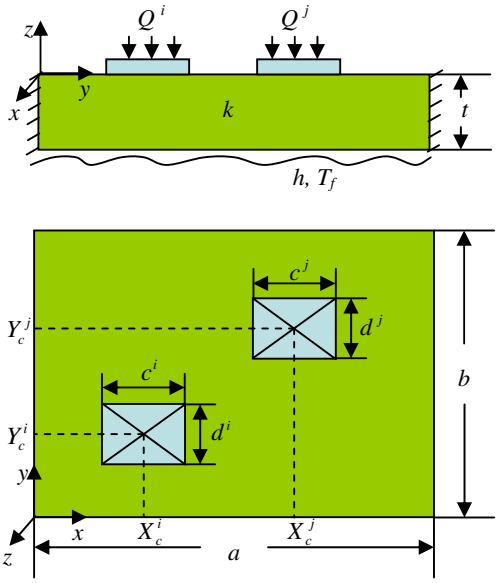

Fig. 1. Schematic diagram of side by side multi-chip package.

$$\nabla^2 T = \frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0, \tag{1}$$

with boundary conditions,

$$\left.\frac{\partial T}{\partial z}\right|_{z=0} = -\frac{1}{k}\sum_{i=1}^{N}\frac{Q^i}{A_s^i}, \tag{2}$$

$$\left.\frac{\partial T}{\partial z}\right|_{z=0} = \left.\frac{\partial T}{\partial x}\right|_{x=0,a} = \left.\frac{\partial T}{\partial y}\right|_{y=0,a} = 0, \tag{3}$$

$$\left.\frac{\partial T}{\partial z}\right|_{z=t} = -\frac{h}{k}[T(x,y,t) - T_f], \tag{4}$$

where $T(x,y,z)$ is temperature, T_f ambient temperature, k thermal conductivity, h the convection coefficient, Q^i the power of chip i, and A_s^i the heating area of chip i.

Since the thickness of normal package is very small, the assumption of "no heat transfer across the sides" (i.e. last two of

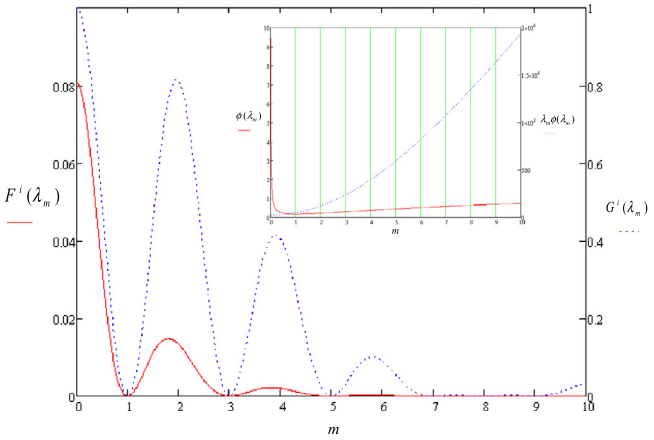

Fig. 2. Function charts of $F^i(\lambda_m)$ (left axis) and $G^i(\lambda_m)$ (right axis) versus m with continuous value. The inset shows the function charts of $\phi(\lambda_m)$ (left axis) and $\lambda_m\phi(\lambda_m)$ (right axis) versus m with continuous value. The green lines indicate the integers of m. It can be seen that although the values of $\phi(\lambda_m)$ are comparable for each m, the $\lambda_m\phi(\lambda_m)$ rapidly increases with m. The rapidly increasing property suppresses the peaks of $G^i(\lambda_m)$, so that only first few terms of $F^i(\lambda_m)$ are needed to be considered. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)