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A study of the interaction of gallium arsenide with wet chemical formulations using thermodynamic calculations and spectroscopic ellipsometry

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ABSTRACT

This paper investigates the effectiveness of different wet chemical treatments and their ability to produce/regrow a thin, stable surface oxide layer on GaAs. Results from thermodynamic considerations indicate that a stable surface oxide layer, free of excess arsenic and arsenic oxides, can be achieved by properly choosing aqueous solutions targeted within the GaAs solubility range ($pH < 3$ or $pH > 11$) followed by deionized (DI) water rinsing. This is further corroborated by spectroscopic ellipsometric data that can qualitatively, but correctly, identify the thickness of the surface oxide layer after different wet chemical treatments. Specifically, samples treated with acidic solutions based on HCl, HF, and H_3PO_4 and diluted ammonium hydroxide solution produce a more stable surface layer that is thinner than the native oxide layer on GaAs. The results and subsequent discussion are presented in the context of an attempt at achieving a well passivated GaAs surface, free of excessive surface state defects responsible for Fermi-level pinning.

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1. Introduction

The past 50 years of IC technology has driven semiconductor manufacturing to aggressively scale CMOS devices close to their performance limits. The end of the roadmap for Si-based CMOS devices will most likely occur at the 22 nm technology node; however, a consensus among the community has not yet been reached on the possible candidate technologies that could serve as a suitable replacement [1]. As part of this consideration, it is pointed out that CMOS has utilized Si as the substrate not because it is the best semiconductor, but because of its high quality oxide (SiO_2) and well passivated surface. Since this intrinsic oxide was recently replaced with a high-k oxide offering superior device scaling characteristics [2], efforts now look towards improving CMOS device performance by choosing a substrate channel with better characteristics than that of Si. Gallium arsenide-based materials offer numerous advantages over Si due to their high electron mobility (~5× that of Si), high breakdown fields, semi-insulating substrate, and direct bandgap. In turn, these material characteristics allow a faster CMOS logic operation, provide a platform for higher power/temperature applications, prevent cross-talk during high frequency operation, and offer more versatility towards a wider range of device applications, respectively.

However, considerable research efforts over the past three decades have identified an intrinsic disadvantage of GaAs surfaces that has yet to be completely mitigated. Under ambient conditions, GaAs is known to have a native oxide that is not water-soluble and is not easily passivated by hydrogen (unlike silicon). Several groups have demonstrated that the Fermi-level (E_f) is easily pinned near midgap for such non-reconstructed surfaces [3–7]. In addition, Fermi-level pinning has proved invariant with respect to surface coverage (e.g., less than one monolayer of adsorbed oxygen was found to pin E_f) or adsorbed/deposited species (O_2, metal, etc.); all of the above scenarios pinned E_f at the same midgap energy.

Eventually a consensus was reached that attributed the surface Fermi-level pinning of GaAs to an excess of As_{Ga} anti-sites (i.e., an As atom on a Ga site) at the surface that induces surface states in the bandgap [7]. Since the surface Fermi-level is always pinned at the same energy, regardless of adsorbed species coverage, the effect is considered indirect and associated with a surface lattice imperfection. The solution, therefore, to inhibit Fermi-level pinning is to prevent amorphization of the interface and keep the reconstructed surface stable and free of excess As.

Since the work detailed in Ref. [7], several groups have focused on different methods to clean and passivate the GaAs surface in an attempt to provide a high quality, thermodynamically stable insulator that will minimize the density of surface states (similar to SiO_2 on Si). This challenge serves as the main obstacle towards III–V based CMOS logic applications since experimentally observed

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consequences such as capacitance–voltage (*CV*) frequency dispersion, an inability to tune flatband voltage (V_{fb}), excess leakage current, as well as high interface trap density (D_{it}) can all, ultimately, be traced back to Fermi-level pinning. Wet chemical treatments using inorganic sulfides (Na_2S and $(NH_4)_2S_x$) or alkaline ammonia sulfide solutions have demonstrated the ability to leave the GaAs surface un-pinned (although, still with high D_{it} values) by producing a sulfide passivated layer [8–15]. However, these organic sulfur compounds can be extremely toxic and may not be a viable manufacturing option. Potential wet chemical treatments that can be implemented into a manufacturing environment include dilute inorganic acids such as HCl, HF, or H_3PO_4, dilute alkali (NH_4OH), and dilute peroxide solutions [16]. Two potential solutions to remove elemental As and leave a near stoichiometric surface are HCl followed by dilute ammonium hydroxide and ammoniacal solutions with a high H_2O_2 content (20% ammonia, 50% peroxide, and 30% water).

Considerably more focus is needed in mitigating the presence of surface states for GaAs to extend the CMOS roadmap beyond Si-based devices. However, to be successful at engineering or developing the correct process that can deliver a thermodynamically stable oxide interface with a low surface state density, advanced characterization and metrology methods must be available that can identify and facilitate an understanding of how the surface (and charge state) is impacted by subsequent wet chemical treatments. The above mentioned studies primarily relied upon photoluminescence spectroscopy (PLS) or X-ray photoelectron spectroscopy (XPS) to extract surface-sensitive information pertaining to surface state defects or atomistic structure and stoichiometry, respectively. Alternatively, electrical CV measurements can be used after device fabrication, but they provide only a quantitative insight into what processes induce Fermi-level pinning. These measurements do not provide any physical insight into the atomistic mechanism originating at the interface that is responsible for the observed electrical response and are confounded by subsequent dielectric and metal deposition steps, as well as thermal anneal processes necessary for complete device fabrication. This report focuses on thermodynamic calculations to first identify prospective wet chemical treatments, followed by a DI water rinse, that may be able to remove excess As and As-oxide species, thus leaving a desired Ga_2O_3 on the surface. With the assistance of Pourbaix diagrams optimal pH conditions can be identified that facilitate arsenic and gallium solubility in water. Additional calculations were done to elucidate how the oxidizing solution potential affects the stability of GaAs. Based on these thermodynamic considerations and previous literature reports, nine different wet chemical treatments were then identified as potential candidates to yield a well passivated GaAs surface free of elemental As. The nine different cleaned samples were then measured using spectroscopic ellipsometry (SE) to characterize the effectiveness of the wet chemical treatment and tentatively identify candidate solutions that produce thinner surface oxides of varying stoichiometry.

2. Experimental methods and considerations

It is reported that the surface film of GaAs under ambient conditions is likely to consist of gallium oxides (Ga_2O and/or Ga_2O_3) and arsenic oxides (As_2O_3 and/or As_2O_5) [17]. Fig. 1 presents the results of calculations of the free energy change for the oxidation of Ga and As in one atmosphere of oxygen at different temperatures. Since it was difficult to find reliable thermodynamic data for Ga_2O (s), calculations are presented for only the formation of Ga_2O_3, As_2O_3 and As_2O_5. It is evident from this figure that oxidation of these elements is thermodynamically favorable (in the temperature range of 25 °C–900 °C). Additionally, arsenic oxide is also

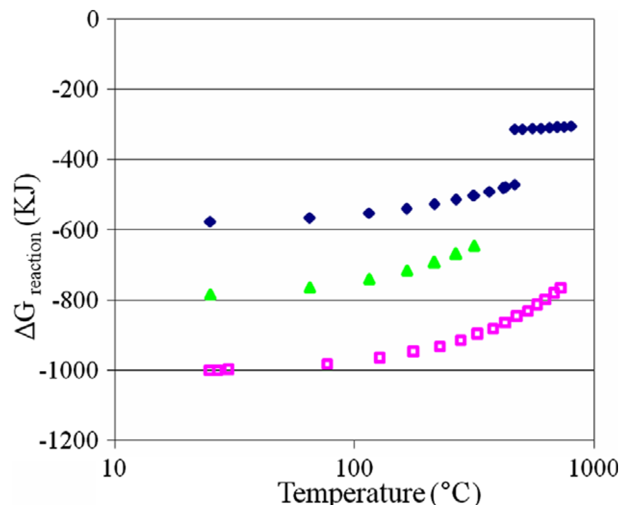
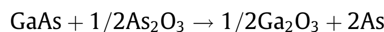


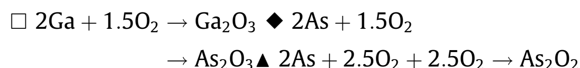
Fig. 1. Free energy change during oxidation of Ga and As in 1 atm of oxygen as a function of temperature.

found to be unstable when in contact with GaAs and is likely to reduce to elemental As. Indeed, the free energy change is ~−105 kJ/mol at 298 K according to the following reaction:



$$GaAs + 1/2As_2O_3 \rightarrow 1/2Ga_2O_3 + 2As$$

This suggests, in light of previous findings identifying excess As as the main contribution to Fermi-level pinning [7], that the ideal wet chemical treatment of an oxidized GaAs substrate should be engineered to target the removal of excess As (and not the arsenic oxides).



□ $2Ga + 1.5O_2 \rightarrow Ga_2O_3$ ◆ $2As + 1.5O_2 \rightarrow As_2O_3$ ▲ $2As + 2.5O_2 + 2.5O_2 \rightarrow As_2O_2$

Selecting the suitable aqueous solution to remove excess As can be facilitated with the use of a Pourbaix diagram. A Pourbaix diagram for the Ga–As–water system drawn for a gallium activity of 10^{-6} and arsenic activity of 10^{-4} is shown in Fig. 2. The diagram was constructed using STABCAL software with thermodynamic data published by NBS. It is clear from this diagram that arsenic is soluble in the entire pH range; at acidic pH values arsenous acid (H_2AsO_3) and arsenic acid (H_3AsO_4) are stable and at alkaline pH values anions of these acids are stable. In contrast, exposure of GaAs to aqueous media is likely to produce soluble gallium species

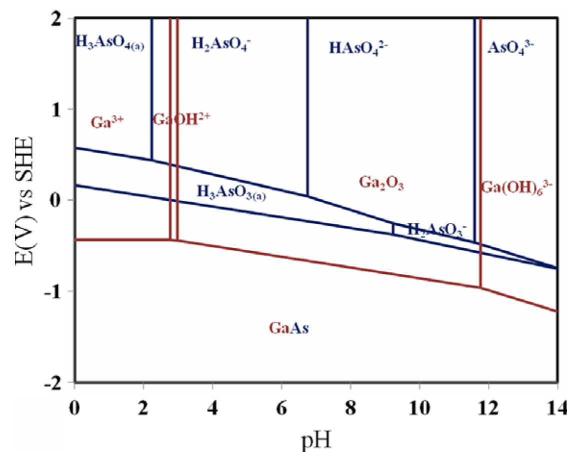


Fig. 2. Pourbaix diagram of Ga–As–H_2O system (activity Ga = 10^{-6}; As = 10^{-4}).

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