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Introductory Invited Paper

Real-time soft-error rate measurements: A review

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ABSTRACT

The real-time (or life testing) soft-error rate (SER) measurement is an experimental reliability technique to determine the soft error sensitivity of a given component, circuit or system from the monitoring of a population of devices subjected to natural radiation and operating under nominal conditions. This review gives a survey over recent real-time SER experiments, conducted in altitude and/or underground, and investigating modern CMOS logic technologies, down to the 40 nm technological node. The review also includes our different contributions conducted during the last decade on the ASTEP Platform (Altitude Single Event Effects Test European Platform) and at the LSM facility (Underground Laboratory of Modane) to characterize soft error mechanisms in advanced static (SRAM) memories. Finally, the review discusses the specific advantages and limitations of this approach as well as its comparison with accelerated tests using intense particle beams or sources.

1. Introduction

The increasing sensitivity of modern electronics to natural radiation, in the terrestrial environment and especially at ground level, is clearly becoming one of the major concerns in reliability issues. Schematically, two main types of natural radiation are able to induce soft errors in circuits at ground level: (i) the atmospheric particles and primarily the neutrons that are produced by collisions of cosmic rays with the earth's atmosphere; (ii) the alpha particles emitted by radioactive impurities that are present in low concentrations in package and IC materials [1,2]. For neutrons, a distinction can be made between low energy (i.e. thermal) neutrons only interacting with the ^{10}B isotope of boron eventually present in circuit materials and high energy neutrons (>1–10 MeV) indirectly ionizing the matter via elastic or inelastic collisions with target nuclei. Thermal neutrons are no longer responsible of the majority of soft errors in modern CMOS technologies [3] since semiconductor processes have completely eliminated the presence of ^{10}B in Borophosphosilicate glasses (BPSG) used in the back-end-of-line (BEOL), or outright the use of the BPSG itself, considered as the principal reservoir of ^{10}B and the dominant source of boron fission in circuits [4] (however, ^{10}B can also subsist within the BEOL structure, for example as a coating over tungsten plugs [5]).

To predict the impact of these radiation constraints on the behavior of electronics and to quantify its radiation-induced error rate, called the soft error rate (SER), different experimental approaches can be used [1]. The present paper reviews and discusses the so-called "real-time" method or "life testing", an experimental reliability technique to determine the soft error sensitivity of a given component, circuit or system from the monitoring of a population of devices subjected to natural radiation and operating under nominal conditions. The fact that natural radiation is considered in real-time testing instead of artificial sources offers the guaranty to characterize the "true" SER of the circuit under test in the terrestrial radiation environment. But, as we will shown later in this paper, such an estimation has a certain "price", notably in terms of experiment duration, logistic and cost. One of the objectives of this review is precisely to survey all these aspects of the technique and to give an up-to-date overview about the most recent works in the domain. The paper is organized as follows.

After briefly introducing the different methods of SER measurements in Section 2, we will focus in Section 3 on the real-time methodology and challenges, focusing on the most important key-points for this approach in terms of test equipment and procedure, experimental constraints and radiation environment metrology. In Section 4, we will survey different works published in the recent literature investigating with this technique the soft error occurrence in various modern CMOS technologies, from 0.25 μm

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down to 45 nm technological nodes. Section 5 will summarize our own contributions conducted during the last decade on the ASTEP Platform and at the LSM facility to characterize soft error mechanisms in advanced static (SRAM) memories, covering 130–40 nm CMOS technologies. Finally, in Section 6, we will discuss the specific advantages and limitations of this approach as well as its comparison with accelerated tests using intense particle beams or sources.

The paper will refer frequently to the JEDEC standard 89A [6], which defines, for the microelectronics industry, the standard requirements and procedures for terrestrial SER testing of integrated circuits and reporting of results. We will try to follow the terms and definitions introduced in this standard.

2. Experimental methods to measure the soft error rate

Different experimental approaches can be considered to estimate the SER of a given device, circuit or system. The first one, called "field testing", consists in collecting errors from a large number of finished products already on the market. The SER value is evaluated a posteriori from the errors experienced by the consumers themselves; it takes generally several years after the introduction of the product on the market. Measurement on production circuits or systems poses significant challenges since the measurement must not introduce any noticeable performance impact on the existing running applications [7]. This method is not adapted to upstream reliability studies performed during the cycle of product development and will not be considered in the following.

The second approach is based on accelerated tests using intense particle beams or sources chosen for their capability to mimic the terrestrial neutron spectrum or to generate alpha particles within the same energy range than the alphas emitted by radioactive contaminants. This accelerated SER (ASER) method is fast (data can be obtained in a few hours or days instead of months or years for the other methods), a priori easy to implement and only requires a few functional chips to estimate the SER. This allows the manufacturer to perform such radiation tests relatively early in the production cycle. Another major and growing advantage is its capability to quantify from a very large statistics (cumulated number of events) the importance of multiple cell/multiple bit upsets in the radiation response of ICs fabricated in technological nodes typically below 65 nm. But data can be potentially tainted by experimental artifacts (more or less well controlled according to the facility, the experimental setup or other various experimental conditions). As a direct consequence, ASER results must be extrapolated to use conditions and several different radiation sources must be used to ensure that the estimation accounts for soft errors induced by both alpha particle and cosmic-ray-neutron events. We will discuss these issues in Section 6.

The last approach, called "real-time" SER (RTSER) or "life testing", can be considered, in a certain way, as a middle path of the two previous approaches. As in field testing, the method considers a large population of circuits working in the natural radiation environment and, as in accelerated testing, at least for neutrons, the intensity of the natural radiation can be increased by deploying the test in altitude. However, the acceleration factor has nothing to do with those of the accelerated tests. Considering an equivalence of the radiation background composition in altitude and at sea-level (this point will be discussed in Section 3), typical values between 5 and 20 as a function of the test location on Earth, can be reached. Devices have thus to be tested for a long enough period of time (months or years) until enough soft errors have been accumulated to give a reasonably confident estimate of the SER. As preconized by the JEDEC standard 89A [6], the term accelerated should be reserved for intense radiation sources that do not occur in natural terrestrial environments. System SER is another term that is often used and is considered synonymous with real-time SER. Real-time testing has the major advantage of being a direct measurement of the actual product SER requiring no intense radiation sources, extrapolations to use conditions, etc. [6]. However, real-time testing does require an expensive system capable of monitoring hundreds or thousands of devices in parallel, for long periods of time. All these aspects will be described and discussed in details in the following sections.

Fig. 1 summarizes the different ways to evaluate the SER in the form of a two-dimensional chart, highlighting test specificities of each approach. Of course, such information is only indicative but this figure has the merit to clearly show fundamental differences between RTSER and ASER test strategies, notably in terms of test duration, number of devices, test cost, test setup complexity and experimental artifacts.

3. Real-time testing methodology

The primary objective of a RTSER test is to obtain a well-defined estimation of the total soft error rate for the component/circuit under test and, ideally, to determine the respective contributions of the different radiation constraints in this failure rate. SER being generally (extremely) low at ground level, the methodology consists in a direct observation of a (very) large number of devices working in parallel under standard operating conditions and exposed to ambient background radiation. We examine in the following several key-points of the RTSER test methodology, including some instrumentation issues, the different ways to separate the SER components and the importance of radiation background metrology for the accurate estimation of the SER.

3.1. Instrumentation issues

In RTSER experiments, the role of the automatic test equipment (ATE) is crucial in the detection and identification of errors related to the population of devices under test. Because soft errors can be considered as "rare events" in such a real-time approach (precisely due to the weak natural radiation constraint), the design of this ATE is technically complex to be sure that both the hardware and the software do not introduce any artifact or wrong error during the process of detection and counting of soft errors. Moreover, the number of chips involved in the experiment must be as large as possible to reach a satisfactory statistics in a reasonable duration; this also introduces additional difficulties in terms of setup complexity, power management, cost and test operation.

Fig. 2 (top) shows a RTSER setup illustrating the different parts of a typical ATE [8]. The circuits to test (packaged devices) are assembled on one or different IC printed boards. A modular configuration composed of several daughter boards connected to motherboards is privileged to offer the possibility to replace/isolate faulty devices during the test or to reuse the setup for other circuits. Another advantage is to use the same core tester with a single daughter card for accelerated tests. The test control is performed by the test processor for lower level functions (memory array write/read, data comparison, current and voltage monitoring) and by the control software for higher-level functions (selection of test conditions, generation of data pattern, test flow sequencing, data processing) [1]. Fig. 2 (bottom) shows a screenshot of the main page of the control software specially developed for the ATE detailed above [8]. Different windows and graphs allow the user to visualize in real-time the most important test parameters, control and monitoring signals, in particular the card temperatures, the voltage stability and power current consumption. The PC provides network connection, time stamping and data storage