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Flexible substrate compatible solution processed P-N heterojunction diodes with indium-gallium-zinc oxide and copper oxide

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ABSTRACT

Printed electronics on flexible substrates requires low temperature and solution processed active inks. With n-type indium-gallium-zinc oxide (IGZO) based electronics maturing for thin film transistor (TFT), we here demonstrate its heterojunction diode with p-copper oxide, prepared by sol-gel method and processed at temperatures compatible with polyimide substrates. The phase obtained for copper oxide is CuO. When coated on n-type oxide, it is prone to develop morphological features, which are minimized by annealing treatment. Diodes of p-CuO films with IGZO are of poor quality due to its high resistivity while, conducting indium-zinc oxide (IZO) films yielded good diode with rectification ratio of 10^4 and operating voltage <1.5 V. A detailed measurement at the interface by X-ray photoelectron spectroscopy and optical absorption ascertained the band alignment to be of staggered type. Consistently, the current in the diode is established to be due to electrons tunnelling from n-IZO to p-CuO.

1. Introduction

Transparent and flexible devices on a variety of substrates that involve low cost fabrication processes, such as printing and roll to roll fabrication, are imminent. They are likely to use oxide semiconductors [1–4]. Inorganic oxide such as n-type indium gallium zinc oxide (IGZO) semiconductor has already found commercial use, especially in fabricating display backplanes on account of higher carrier mobility in transistors than with amorphous silicon [5,6]. Because of amorphous nature of these oxide materials, they can be deposited onto any substrate and are excellent for stacked structures. In addition to that, availability of easy solution processing methods for their processing could drastically reduce the cost [5,7–9]. However, low temperature fabrication and compatibility with flexible substrates was a major challenge which solution processing had faced in the past few years, but recently new alternative annealing methods such as photochemical activation [10,11], oxygen plasma treatment [12], self-heating reactions [13,14], high pressure annealing [15] etc. has been effectively utilized for the dramatically lowering of the processing temperature [16].

In order to take the full benefit of oxide semiconductors and to form complementary metal oxide semiconductors (CMOS) circuits, it is important to realize a suitable p-type material with comparable performance and cost effective means. Apart from transistors, p-n junction diode is also an important component in such circuits, although Schottky diodes with sputtered IGZO and Pt have been made [6,17–19]. In case of Si based technology, bulk doping is possible, hence formation of homojunction can easily be realized. However, such junctions are not possible with oxide semiconductors, since the conductivity variation is mainly governed by the formation of vacancies and only one type, n- or p-type, conductivity is seen in films deposited under practical oxygen pressures. Thus, for fabricating a junction diode, an alternative is to form a heterojunction of p-type and n-type material. N-type semiconducting behaviour can profoundly be seen in most of the oxide semiconductors; IGZO, or its variant, is the most common example. Due to the presence of non-directional metal "ns" orbitals in the conduction band minimum (CBM), they offer large mobility values [2]. However, unavailability of suitable p-type inorganic oxide semiconductor materials with comparable performance is because of presence of highly directional localized 2p orbitals from oxygen in valence band maximum (VBM) and deep level traps near VBM, thereby limiting the holes mobility [20]. Early, reports suggests that using hybridized orbitals between Cu *3d* and O *2p*, p-type semiconducting behaviour can be seen in $CuAO_2$ (A = trivalent cation) for example: $CuAlO_2$, $CuScO_2$ and $CuCrO_2$ [21–24]. However, no transistor action has been reported with these materials, possibly due to very low holes mobility [22]. Later on, high performance ($\mu > 1\ cm^2/Vs$) p-type oxide based transistors could be achieved with SnO, NiO and copper based oxides such as cupric oxide (CuO) and cuprous oxides (Cu_2O) [22,25–27]. Among these

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copper based oxide has been reported to possess highest hall mobility, of the order of 10^2 cm^2/Vs, and inherent p-type behaviour, due to the presence of negatively charged copper vacancies [28,29]. Apart from the transistor application, heterojunctions of copper based oxides have also been reported in heterojunction solar cells and gas sensors [30–36]. Out of the two phases of copper oxide, CuO phase is stable in comparison to Cu_2O, as the latter has a tendency to oxidize to CuO phase. Also, obtaining Cu_2O is difficult and requires fine tunability of oxygen partial pressures [26].

Here, objective of our work is (a) to fabricate a p-n junction diode with solution processing, where both n-type and p-type materials are processed through a similar methodology, (b) to fabricate a p-n junction diode at low temperature, preferably below 350 °C, so as to meet the requirements of flexible substrates such as polyimide and (c) to fabricate a p-n junction diode in which both n and p type materials should preferably be amorphous so that the interfacial states can be minimized. In order to fulfil these, an attempt has been made to fabricate low temperature p-n junction diode using solution processing approach with IGZO, IZO as n-type and CuO as p-type semiconductors.

2. Experimental

In order to prepare IGZO and IZO sol of compositions S1 (In:Ga:Zn: 1:1:1), C1 (In:Zn: 3:1) and C2 (In:Zn: 5:1), zinc acetate dihydrate [Zn $(CH_3COO)_2{\cdot}2H_2O$], gallium nitrate hydrate [Ga $(NO_3)_3{\cdot}xH_2O$] and indium nitrate hydrate [In $(NO_3)_3{\cdot}xH_2O$] were taken as the precursor materials. Sol with molarity (0.5 M) was prepared by dissolving appropriate amount of precursor material in 5 ml of 2-methoxyethanol followed by addition of monoethanolamine, which acts as stabilizer. Few drops of acetic acid were also added to make the solution homogeneous. The solution was then kept at 60 °C with constant stirring for 2 h. 1 M sol of copper oxide sol was also prepared by the same route as discussed above using copper acetate monohydrate [Cu $(CH_3COO)_2{\cdot}H_2O$] as the precursor material. All the precursor materials used were from Aldrich chemicals. Sols of compositions S1, C1 and C2 were spin coated at 3000 rpm while CuO sol was spin coated at 1000 rpm on glass and ITO coated glass substrates of size $1'' \times 1''$; the corresponding final thicknesses of these films after annealing treatment, as measured using thickness profilometer (Dektak XT- Bruker), are listed in Table 1. These thicknesses closely match with those estimated from cross section images of the films using field emission scanning electron microscope (FESEM) (see Fig. S1, in the Supporting information).

For device fabrication, the ITO coated substrates were first cleaned with a soap solution followed by RCA (Radio Corporation of America) bubble cleaning. The ITO surface was ozonized to make it hydrophilic, necessary for obtaining good uniform thin films. Four types of diode structure, labelled D1-D4, are prepared, according to the list in Table 2; in all cases, first the n-type layer is spin coated on the substrate, followed by the p-type layer and copper contact at the top. Each layer after spin coating undergoes a prebake, followed by annealing, along with optional intermediate ultraviolet (UV) curing as a separate step. For prebaking, n-type layers are subjected to 200 °C while p-type layers to 150 °C, for 0.5 h in each case. The D1 and D2 diodes are prepared by using IGZO as n-type semiconductor. In case of D1 diode the IGZO films are annealed at 400 °C for 2 h, while IGZO in D2 diode is subjected to additional UV curing (Novascan PSD series) in nitrogen environment for 2 h after prebaking and subsequently annealed at a lower temperature of 325 °C for 2 h, to make them compatible with flexible substrate. The D3 and D4 diodes are prepared by using IZO as n-type semiconductor with IZO (C1) and (C2) compositions respectively. The IZO films are processed in conditions similar to that of IGZO films in D2 diode. The p-type CuO layer coated on n-type films, after prebaking, is annealed at 450 °C for 0.5 h for D1 diode and at 250 °C for 1 h in D2, D3 and D4 diodes.

After CuO layer, Cu electrodes of 1.5 mm diameter were deposited on these samples using a thermal evaporator.

Resistivity of IGZO and IZO thin films on glass were measured using Van der Pauw configuration, with the help of Keithley 6517A high resistance electrometer and Keithley 220 current source meter, while resistivity of copper oxides were measured using four probe method. I-V characteristics of ITO/IZO/CuO/Cu hybrid diode structure was taken with the help of Keithley 2602 system source meter.

Table 1
Compositions of spin-coated precursor films and their final thicknesses.

Material	Composition	Molarity	Thickness
IGZO	S1 (In:Ga: Zn: 1:1:1)	0.5 M	40 ± 2 nm
IZO	C1 (In:Zn: 3:1)	0.5 M	40 ± 2 nm
IZO	C2 (In:Zn: 5:1)	0.5 M	40 ± 2 nm
Copper Oxide	Pure phase	1 M	125 ± 2 nm

3. Results and discussion

In order to fabricate n-p heterojunction diode, we select a common composition of n-IGZO as (In:Ga:Zn: 1:1:1), n-IZO as (In:Zn: 3:1 or In:Zn: 5:1) and p-type copper oxide. The goals in this work are to demonstrate (a) a diode with solution processability of the semiconductors, (b) temperature compatibility with substrates for flexible electronics, specifically polyimide, even though the development may be on glass and (c) that preferably both the types of semiconductors are amorphous in order to minimize the interface states.

The oxides of copper mainly exist in two stable forms namely cuprous oxide (Cu_2O) and cupric oxide (CuO). For solution processed copper oxides, Cu_2O phase generally emerges when processed at low temperatures. However, it can easily get oxidized to CuO, unless there is a fine control of the oxygen partial pressure [26]. In addition, CuO has been reported as more suitable candidate for the diode application, mostly in solar cells, as compare to Cu_2O [37]. The p-CuO films cast from the sol-gel method are generally crystalline, especially those annealed at high temperatures. Hence, in order to minimize interface defects in n-p hetero-junction diodes, at least the n-type material should preferably be amorphous, such as IGZO. In addition, selecting IGZO and IZO as n-type semiconductor allows us to remain on a recently emerged platform of these semiconductors, which are now already in commercial use.

3.1. N-type semiconductor films

We first examine the n-type semiconductor films of IGZO and IZO, both spun from a freshly prepared sol on the glass substrate. We begin with IGZO film corresponding to D1 diode in Table 2; the film is of composition S1 (Table 1). After coating, typically these films are annealed at approximately 400 °C for 2 h [38–39]. However, in order to obtain a good quality pin-hole free film, an intermediate step of pre-annealing at 200 °C for 0.5 h was incorporated. The crystallinity of this film is examined by comparing grazing angle (0.5°) X-ray diffraction with that of the glass substrate (Fig. 1a and b), which indicates an amorphous phase, as desired for minimizing the interface states.

At a micro level scale, examined through atomic force microscope (AFM) image (Fig. 2a) and phase contrast (Fig. 2b) indicates small morphological features. But, the roughness is only 0.7 nm,