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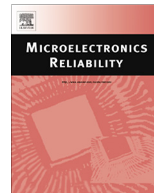

Some aspects on ruggedness of SiC power devices

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A R T I C L E I N F O

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A B S T R A C T

This article is on effects that can destroy SiC power semiconductor devices. The failure physics in SiC devices are discussed based on the well understood effects in silicon devices. In some device properties, such as surge current, short circuit, static avalanche and dynamic avalanche, SiC has significant possible advantages compared to silicon. For cosmic ray stability, there are no unique results. Regarding thermal mechanical stress on interface materials, SiC is more challenging. The same may hold for electrical stress in passivation layers at the junction termination.

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1. Introduction

It is very important for power electronics application to know the effects that can lead to a destruction of semiconductor devices. Knowing the failure limits, one can keep a safety margin in the application. A lot of experience exists with Si, summarized in [1]. Wide bandgap semiconductors are often only discussed regarding their better electrical characteristics and their strong benefit in the application. However, from the viewpoint of system optimization, we must also know the robustness limits.

Table 1 summarizes some basic materials data regarding device ruggedness [1,2]. The interest in new materials has moved from Si to SiC and GaN, and it jumped over GaAs, which, regarding the carrier mobilities, has some advantages and could enable efficient bipolar devices [3]. Regarding the intrinsic density n_i, which is of strong influence to some failure mechanisms, we have a step over 20 decades going from Si to SiC or GaN, respectively.

Meanwhile, SiC is believed to become mature. Problems due to crystal defects (for example bipolar degradation) are not in the focus of this paper. They are overcome or they will be overcome in the next time. The paper do not address reliability aspects on gate oxide degradations (MOSFETs) in SiC, since several groups work on this matter. GaN is not considered in this article, since it is still different to evaluate what is general and which effects can be eliminated by a better technology and a better design. It will be started with failure physics known from silicon, consider the impact of the different parameters in Table 1 on power device failure mechanisms, look to experimental results of SiC devices, and answer the question what is different compared to Si regarding failure physics.

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2. Surge current

Surge current capability is a basic requirement of diodes. To improve the SiC Schottky diode, merged pin-Schottky structures (MPS-diodes) have been introduced [4,5]. Fig. 1 shows the forward IV-characteristics of different SiC Schottky- and MPS diodes, where only characteristic (b) is of a MPS diode where the pin-part becomes active above a current of 20 A. A simplified drawing of a diode with characteristic (b) is given in Fig. 2. Device (a) is a Schottky diode where a potential ring at the edge provides some bipolar injection. Device (c) is an MPS-structure where p-layers do not provide any bipolar injection and behaves like a poor Schottky diode. For device (b), at high current the p^+-regions inject holes. A characteristics like (c) leads to a poor surge current capability.

A surge current pulse for a 4 A 600 V MPS Diode exposed to current pulses of 100 A and 110 A with a pulse time of 500 µs (at half of the current maximum) is shown in Fig. 3. Visible is a strong voltage increase due to extreme self-heating and the resulting decrease of the carrier mobilities. After the surge current pulses, the blocking characteristic was controlled. Some devices had an instable blocking behavior. Opening some of these devices showed that molten Al shoot out across the junction termination (Fig. 4). This is a clear indication for temperatures far above the melting temperature of Al. A thermal simulation with a rough grid indicated that temperatures above 1000 °C should have occurred. Nevertheless, the semiconductor body was unaffected. This result proves that the SiC semiconductor material is extremely temperature stable. The reason for the possible high ruggedness is the low n_i that makes SiC very rugged. With Si, at high temperatures the intrinsic carrier generation becomes dominant [1], and with intrinsic carrier generation and temperature exists a positive feedback. This is one of the effects that limit surge current capability. With SiC, we are far away from significant intrinsic carrier generation.

Challenge for such ruggedness is to make a p-layer with sufficient emitter efficiency, which is more difficult in SiC due to

Table 1
Some ruggedness-relevant data of Semiconductor materials, $T = 300$ K [1,2].

	Si	GaAs	4H–SiC	GaN
Bandgap [eV]	1.124	1.422	3.23	3.39
Intrinsic density n_i [cm^{-3}]	10^{10}	10^7	10^{-10}	10^{-10}
Critical field strength [V/cm]	2×10^5	4×10^5	2×10^6	$>3 \times 10^6$
Electron mobility μ_n [cm^2/Vs]	1420	8000	1000	<1000 2000[a]
Hole mobility μ_p [cm^2/Vs]	470	400	115	<200
Thermal conductivity [W/mm K]	0.13	0.055	0.37	0.13

[a] 2D electron gas.

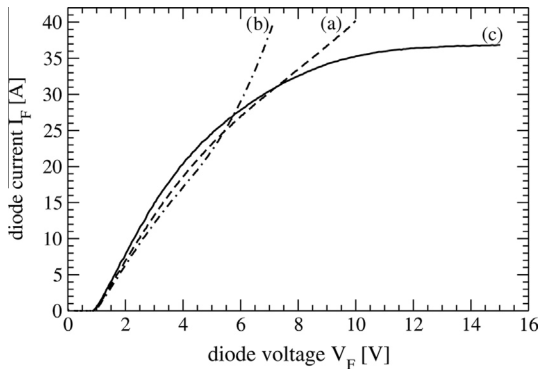

Fig. 1. Forward characteristic of SiC Schottky- and MPS diodes. Fig. from [5].

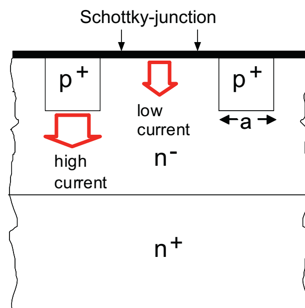

Fig. 2. MPS diode with injection of holes at high current density.

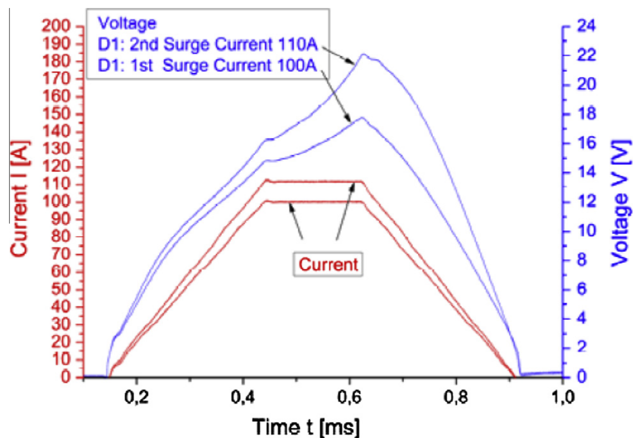

Fig. 3. Surge current measurement of a SiC MPS diode rated 4 A 600 V at an initial temperature of $T = 25$ °C. Fig. from [6].

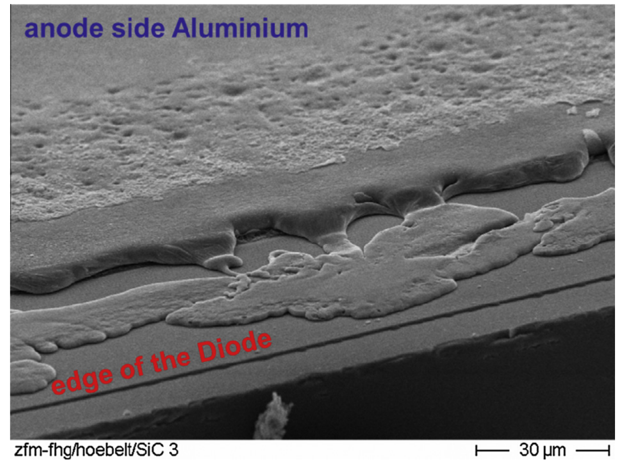

Fig. 4. SEM picture of a MPS diode after a destructive surge current pulse, molten metallization. Fig. from [6].

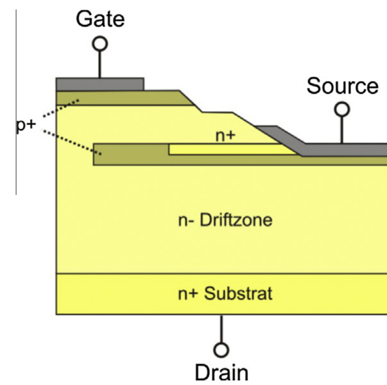

Fig. 5. Structure of a SiC JFET, normally-on type.

incomplete ionization of acceptors. A further condition is that the lateral width a of the p-layers (Fig. 2) is not to small, since the lateral voltage drop below the p$^+$-regions must exceed the junction voltage (approx. 2.8 V at 300 K) to start hole injection from the p$^+$-regions.

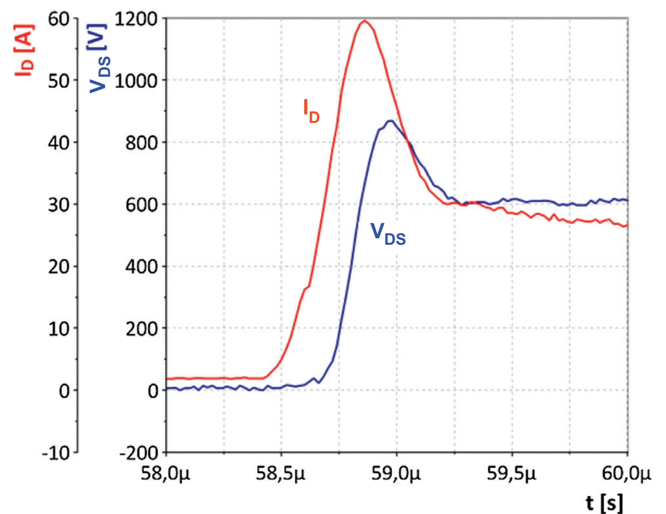

Fig. 6. SCII event with a 5 A 1200 V JFET, $T = 21$ °C, initial phase of the SC.

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