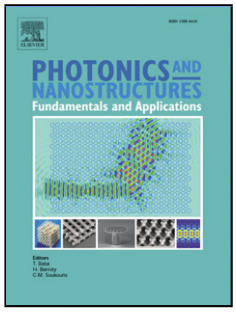

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Theoretical Designs for Novel Photonic Crystal Nanocavities with Si (111) Interfaces

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Highlights

- A New pattern for Photonic Crystals requiring only self-limited Fabrication process is investigated.
- The Design of this new photonic pattern relies on the Silicon anisotropic structure allowing uniform morphology interfaces.
- Overcome of actual miscellaneous Fabrication Process lapsing unintended corrugation artefacts.
- Affordable cost of wet-etching technique feasible to mass produce atomically flat on cheap optical components.

***Abstract*—We designed a series of photonic crystal (PhC) nanocavities using atomically flat silicon (111) interfaces and examined the impacts of the surfaces on the optical confinement. The nanocavities were simulated using the 3D finite-difference time-domain method and assessed against existing PhCs. Despite the design restrictions, we showed that a *Q* value up to 115,800 and *Q/V* values of 10^3-10^5 λ^{-3} are achievable without further design optimization. The results suggest that silicon (111) surfaces can be used for fabricating PhC nanocavity-based devices in a practical and economical way with high manufacturing tolerance and increased repeatability.**

***Index Terms*—Etching, nanofabrication, photonic crystals, silicon-on-insulator**

I. Introduction

With small footprints and low energy consumption reaching the order of fJ/bit, photonic crystals (PhCs) offer us a prospect of all-optical circuits, devices and interconnects in the future [1]. One remarkable feature of the PhC is its ability to confine light within nanocavities as an effect of both distributed Bragg reflection and internal reflection [2], [3]. Nanocavities with ultra-high quality factors and extremely small mode volumes have been successfully applied to both active and passive devices, such as lasers [4]–[6], light-emitting diodes (LEDs) [7], [8] and switches [9], [10], transforming PhCs into essential building blocks for future optical devices.

PhCs are compatible with existing Complementary-Metal-Oxide-Semiconductor (CMOS) fabrication processes, but they are very sensitive to structural disturbances caused by line-edge roughness [11]–[13]. The conventional PhC slab is a triangular lattice of air holes in a dielectric slab and it remains a huge challenge to fabricate them with the very high accuracy of the order between 1 to 10 nm in a repeatable way [14]. Standard optical lithography processes, such as ArF and electron-beam, are known to cause roughness on the sidewalls, even for large feature sizes [15]–[17]. The minimum feature size of PhCs can be below 100 nm and structural disturbances in the atomic scale can have a detrimental effect on their performance, since scattering loss scales proportionally to $(\Delta n)^3$, where Δn is the difference of refractive indices between the slab and the cladding [12], [18]–[20]. The ability to eliminate line-edge roughness would not only minimize scattering losses and improve the performance of the PhC, but also increase the fabrication tolerance, hence the repeatability and reliability of its production, by suppressing contribution to the standard deviation of the patterning position, which current conventional fabrication processes cannot guarantee yet.

One of the effective ways to reduce line-edge roughness is to use the anisotropic alkali wet etching technique [21]. Using an

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