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ScienceDirect
Microelectronic Engineering 85 (2008) 542–547
MICROELECTRONIC ENGINEERING
www.elsevier.com/locate/mee

The interface states analysis of the MIS structure as a function of frequency

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Received 17 July 2007; received in revised form 20 August 2007; accepted 22 September 2007
Available online 29 September 2007

Abstract

The energy distribution of interface states (N_{ss}) and their relaxation time (τ) were of the fabricated the Al/SiO_2/p-Si (MIS) structures were calculated using the forward bias current–voltage (*I–V*), capacitance–frequency (*C–f*) and conductance–frequency (*G–f*) measurements. Typical $\ln[I/(1-\exp(-qV/kT)]$ versus V characteristics of MIS structure under forward bias show one linear region. From this region, the slope and the intercept of this plot on the current axis allow to determine the ideality factor (n), the barrier height (Φ_b) and the saturation current (I_S) evaluated to 1.32, 0.77 eV and 3.05×10^{-9} A, respectively. The diode shows non-ideal *I–V* behaviour with ideality factor greater than unity. This behaviour is attributed to the interfacial insulator layer at metal–semiconductor interface, the interface states and barrier inhomogeneity of the device. The energy distribution of interface states (N_{ss}) and their relaxation time (τ) have been determined in the energy range from $(0.37-E_v)$ to $(0.57-E_v)$ eV. It has been seen that the N_{ss} has almost an exponential rise with bias from the mid gap toward the top of valance band. In contrary to the N_{ss}, the relaxation time (τ) shows a slow exponential rise with bias from the top of the E_v towards the mid gap energy of semiconductor. The values of N_{ss} and τ change from 6.91×10^{13} to 9.92×10^{13} eV^{-1} cm^{-2} and 6.31×10^{-4} to 0.63×10^{-4} s, respectively.
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Keywords: MIS structure; Ideality factor; Barrier height; Interface states; Relaxation time; Frequency dependence

1. Introduction

The metal–insulator–semiconductor (MIS) structures become more and more important in a great variety of fields of modern electronics. The performance and reliability of these structures especially is depend on the formation of insulator layer between metal and semiconductor interface, the interface states distribution between semiconductor and insulator layer, series resistance and an inhomogeneous Schottky barrier contacts. Therefore, the insulator layer must be perfectly homogeneous be deprived of defects such as pin-holes with high dielectric breakdown and present very good Si/SiO_2 interface. In particular, both the interface states density and the fixed charges density must be low. In addition, the reproducibility and the homogeneous of these properties are essential factors for the reliability and the reproducibility of device performances. Moreover, the thickness of insulator layer must be precisely controlled during the fabrication process. This insulator layer is required to prevent the reaction and the inter diffusion at the interface. There are currently a vast number of reports of experimental studies on Schottky barrier heights in a great variety of MS and MIS Schottky diodes [1–9].

During the elaboration of semiconductor devices of the MS and MIS types, defects appear which lead to electronic states with energies located in the forbidden band, the band gap. These states are known as surface states and alter the functioning of such devices. Surface states originate from defects such as dangling bounds at the insulator/substrate interface with energy states in the Si forbidden band gap and are dependent on the chemical composition of the interface [3,10]. The relationship between the admittance

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0167-9317/$ - see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2007.09.008

of the interface state charging process above and the capacitance and conductance of the MIS structure measured in the external circuit has been described and analyzed by Nicollian and Goetzberger [10]. They have observed that the capacitance decreases with increasing frequency. This effect is obtained at low and intermediate frequencies. The interface states can follow the ac signal and yield an excess capacitance, which depends on the relaxation time of the interface states and the frequency of the ac signal. This model can be applied to determine the interface state of a metal-interface layer-semiconductor Schottky diode.

The interface states can affect the C–V characteristics of MIS Schottky diode, causing a bending of the C^{-2}–V plot as well as affecting the ideality factor. In general, a C–V plot shows an increase in capacitance with an increase in forward bias. However, in recent years, wide acceptance has been gained by the capacitance methods of semiconductor investigation, which allows one to obtain extensive information about the parameters of localized electronic states (or energy levels) [3,11–13]. The reason for their existence is the interruption of the periodic lattice structure at the surface [10,13,15], surface preparation, formation of insulating layer and impurity concentration of semiconductor [11]. These interface states usually cause a bias shift and frequency dispersion of the capacitance–voltage (C–V) curves [14].

Furthermore, the C–f and G–f measurements give the important information about the density of the interface states of the structure. This method is called the conductance method in which is accounted for the interfacial layer capacitance. In general, the C–f and G–f plots in the idealized case are frequency independent [3,4,10,16–19]. However, this idealized case is often disturbed due to the presence of an interfacial layer between the contact materials and interface states at the interfacial layer/semiconductor interface [3,10].

The purpose of this paper is determination of interface states density (N_{ss}) and their relaxation time (τ) in Al/SiO_2/p-Si (MIS) structure. The energy distribution of N_{ss} and τ are obtained from experimental the forward bias current–voltage (I–V) and C–V and G/ω–V measurements.

2. Experimental procedure

The Al/SiO_2/p-Si (MIS) structure used in this study were fabricated using boron-doped single crystals silicon wafer with <1 0 0> surface orientation having thickness of 280 μm, 2 in. and 8 Ω cm resistivity. For the fabrication a process, Si wafer was decreased in organic solvent of $CHCICCI_2$, CH_3COCH_3 and CH_3OH consecutively and then etched in a sequence of H_2SO_4 an H_2O_2, 20% HF, a solution of 6 HNO_3:1 HF:35 H_2O, 20% HF and finally quenched in de-ionised water for a prolonged time. Preceding each cleaning step, the wafer was rinsed thoroughly in de-ionized water of resistivity of 18 MΩ cm.

Immediately after surface cleaning, high purity Al metal (99.999%) with a thickness of ~2000 Å was thermally evaporated from the tungsten filament onto the whole back surface of the wafer in the pressure of $\sim 2\times10^{-6}$ Torr in oil vacuum pump system. To form ohmic contacts on the back surface of the wafer, we sintered the evaporated aluminum (Al). The oxidations are carried out in a resistance-heated furnace in dry oxygen with a flow rate of a 2 lt/min and the oxide layer thickness is grown at the temperatures of 650 °C during 60 min. After, following oxidation, the whole back surface of the quarter wafer after etching away the silicon-insulator from the back in HF and then circular dots of ~1 mm diameter and ~2000 Å thick Al contacts are deposited onto the oxidized surface of the wafer for through a metal shadow mask in a liquid nitrogen trapped vacuum system in a vacuum of $\sim 2\times10^{-6}$ Torr. Thus, the Schottky contact is made onto the upper electrode on the insulator with the help of fine phosphor–bronze spring probe. The interfacial layer thickness was estimated to be about 53 Å from measurement of the interface capacitance in the strong accumulation region for MIS Schottky diode [10].

The current–voltage (I–V) measurements were performed by the use of a Keithley 220 programmable constant current source, a Keithley 614 electrometer. The capacitance–voltage (C–V) measurements were performed at various frequencies by the use of HP 4192A LF impedance analyzer (5 Hz–13 MHz). For the C–V measurements, small sinusoidal signal of 50 mV peak to peak from the external pulse generator is applied to the sample in order to meet the requirement [13]. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. Results and discussion

3.1. Current–voltage (I–V) characteristics

The determination of the electric parameters was achieved by using the characteristics formula expressing the current passing through a Schottky diode [1,10,13]

$$I = I_s\left[1-\exp\left(-\frac{qV}{kT}\right)\right]\exp\left(\frac{qV}{nkT}\right) \quad (1)$$

where q and T are the magnitude of electron charge, the temperature in Kelvin, respectively, V_G is the applied voltage, n is the ideality factor and I_s is the saturation current expressed by:

$$I_s = AA^*T^2\exp\left(-\frac{q\Phi_B}{kT}\right) \quad (2)$$

where A is the area of rectifying contact, A^* is the effective Richardson constant and equals to 32 $A\,cm^{-2}\,K^{-2}$ for p-type Si and Φ_B is the barrier height.

The measured of the forward current–voltage characteristics $\ln[I/(1-\exp(-qV/kT)] = f(V)$ of the MIS structure is shown in Fig. 1. The $\ln[I/(1-\exp(-qV/kT)] = f(V)$ curve consist of a linear region, from the slope and y-axis intercept of the linear region yields the ideality factor n

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