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Laterally amalgamated DUal Material GAte Concave (L-DUMGAC) MOSFET for ULSI

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Abstract

In this paper, a novel structure: Laterally amalgamated DUal Material GAte Concave (L-DUMGAC) MOSFET is proposed. The effectiveness of L-DUMGAC MOSFET design was examined by comparing Single Material Gate (SMG) Concave devices with L-DUMGAC devices of various gate length ratios, Negative Junction Depths (NJDs) and metal gate work functions, and it was found that L-DUMGAC exhibits significant enhancement in device characteristics in terms of device efficiency, intrinsic gain, early voltage and the switching characteristics. With the enhancement in device integration technology, the structure offers new opportunities for realizing high performance in the future ULSI production.

Keywords: ATLAS-3D; Concave MOSFET; DMG; Device efficiency; Early voltage; Intrinsic gain

1. Introduction

Enhancement in device integration technology requires rapid scaling of device dimensions to achieve higher speeds and packing densities. As the device miniaturization trend continues, the MOSFET dimensions have advanced into sub-100 nm era, paving the way to various critical issues such as short channel effects (SCEs), punchthrough current, threshold voltage roll-off and hence, resulting in device performance degradation. Concave/grooved gate MOSFETs are considered as one of the promising candidates for suppressing SCEs and improving the hot carrier immunity; and thus the device reliability [1–6]. In this structure, two potential barriers are formed at the concave corners due to high density of electric field lines. Improvement in SCEs is mainly attributed to the formation of these potential barriers. However, carriers in the channel require higher energy to surmount these potential barriers, which limits carrier transport efficiency and hence, current driving capability of the device and transconductance. In order to surmount the problems and further improve the I_{ON}/I_{OFF} ratio, laterally amalgamated DUal Material GAte Concave (L-DUMGAC) MOSFET, as shown in Fig. 1, is proposed. The step potential profile, due to gate electrodes of different metal work functions [7–11], ensures reduction in DIBL and enhancement of carrier transport efficiency and device efficiency (g_m/I_{ds}).

In this paper, the electrical characteristics of L-DUMGAC are compared with SMG Concave MOSFETs in terms of surface potential, V_{th}, DIBL, Sub-Threshold Swing (S), drain current, transconductance, device efficiency g_m/I_{ds}, I_{ON}/I_{OFF}, early voltage, $V_{EA} = I_{ds}/g_d$ and intrinsic gain (A_v). In the first section, an analytical model is developed for the proposed structure and a close proximity of the modeled data with the simulated results authenticates our model. The second section investigates the device characteristics using ATLAS 3D [12], in terms of transconductance, DIBL, Sub-Threshold Swing (S), device

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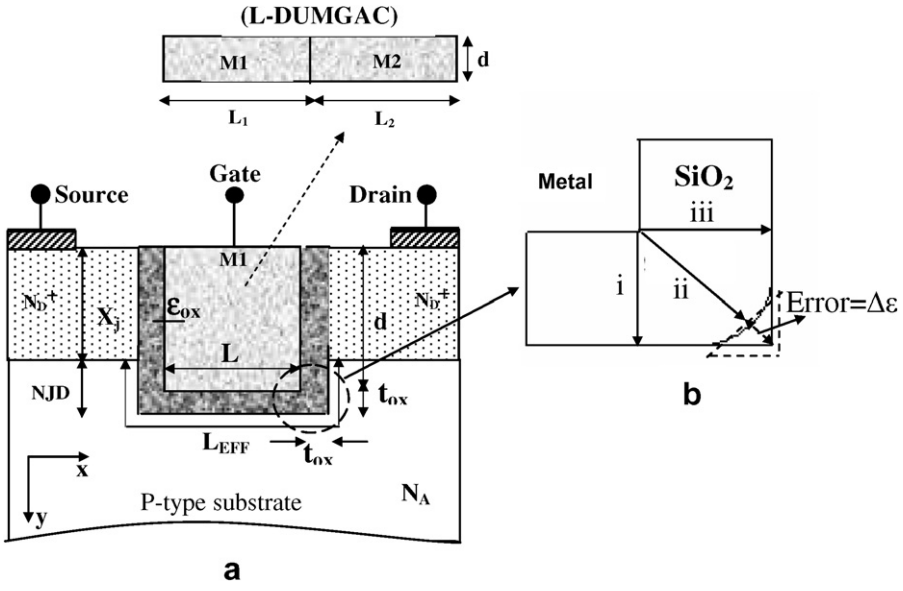

Fig. 1. Schematic structure of Concave MOSFET with L-DUMGAC configuration. Channel length (L) = 50 nm, effective channel length (L_{EFF}) = $L + 2(t_{ox} + NJD)$, device width (W) = 1 μm, groove depth (d) = 100 nm, $L_1 = L_2 = 25$ nm, $N_A = 1 \times 10^{17}$ cm^{-3}, $t_{ox} = 4$ nm, $\varepsilon_{ox} = 3.9$. Work function (Φ_{M1}) = 4.77 V for SMG and for DMG, (Φ_{M1}) = 4.77 V and (Φ_{M2}) = 4.4 V/4.10 V. (b) Schematic representation interpreting the corner effect approximation.

efficiency, I_{ON}/I_{OFF}, early voltage, and intrinsic gain with (a) different Negative Junction Depths (NJDs), (b) different metal gate work functions, (c) same effective lengths and (d) same electrical lengths of the two devices. In our study, we adopt the hydrodynamic energy transport model, which can simulate the non-local transport phenomenon [13].

2. Model formulation

2.1. Two-dimensional potential analysis

A schematic structure of L-DUMGAC MOSFET is shown in Fig. 1. The lengths of metal gates M1 and M2 is L_1 and L_2, respectively. The source/drain (S/D) regions are rectangular and uniformly doped at 10^{20} cm^{-3}. The channel doping concentration N_A is also uniform. The device characteristics were simulated using the ATLAS device simulator [12]. Assuming the impurity density in the channel region to be uniform, the potential distribution $\Phi(x,y)$ in silicon film can be given as [14]

$$\frac{\partial^2\Phi(x,y)}{\partial x^2} + \frac{\partial^2\Phi(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}} \quad \text{for } 0 < x < L_{EFF} \text{ and } (d + t_{ox}) < y < (d + t_{ox} + Y_D) \tag{1}$$

where ε_{Si} is the dielectric constant of silicon, q is the electronic charge, N_A is the substrate doping density, d is the groove depth, Y_D is the depletion layer thickness.

L_{EFF} is the effective channel length which is given by [2]

$$L_{EFF} = L + 2(NJD + t_{ox}) \tag{2}$$

where L is the gate length; NJD is the negative junction depth and t_{ox} is the gate-oxide thickness.

Basic assumption: We have approximated the corner effect in concave structure with an assumption, as shown in Fig. 1(b). In our analysis, the corners have been smoothed out in such a way that i, ii, iii (marked in Fig. 1(b)) are all equivalent to t_{ox} leading to an underestimation of the position of the corner by $\Delta\varepsilon$. It is found that if $\Delta\varepsilon/L_{EFF} < 5\%$, the analytical model results are in close proximity to the simulated results. In our analysis, for NJD = 10 nm with gate lengths varying from $L = 100$ nm to 50 nm, the error $\Delta\varepsilon/L_{EFF}$ varies from 3% to 5%; and for NJD = 30 nm with gate lengths varying from $L = 100$ nm to 50 nm, the error $\Delta\varepsilon/L_{EFF}$ varies from 2% to 3%. In case of gate lengths less than 50 nm, $\Delta\varepsilon/L_{EFF}$ becomes greater than 5% and hence the corner effects in modeling cannot be ignored.

In our analysis, the Poisson's equation has been evaluated in the substrate depletion layer where the channel is virtually depleted of mobile charge carriers. Thus, the potential distribution in the channel, before the onset of strong inversion is governed by the Poisson's equation [15,16] as mentioned by Eq. (1). The Poisson's equation has been considered in the weak inversion region and not in the strong inversion region. This is because if there are any significant mobile charges present in the channel, Poisson's equation becomes non-linear and couples to the continuity equation. Although this problem can be solved by numerical simulations, they can offer only isolated data points and hence do not offer a suitable basis for device models. An analytical solution, however, is necessary to explicate the trends in device behaviour. Restricting the view to the sub-threshold regime makes the solution tractable because Poisson's equation is then linear and decoupled from the continuity equation.

The depletion layer thickness, Y_D is approximately given by