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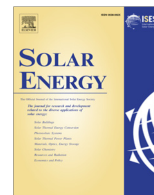

Degradation behavior of crystalline silicon solar cells in a cell-level potential-induced degradation test

Seira Yamaguchi *, Keisuke Ohdaira

Graduate School of Advanced Science and Technology, Japan Advanced Institute of Science and Technology (JAIST), Nomi, Ishikawa 923-1292, Japan

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ABSTRACT

The degradation behavior of crystalline silicon (c-Si) solar cells in a cell-level potential-induced degradation (PID) test and the effect of the test conditions are reported. The PID tests were performed in a vacuum chamber by applying a voltage of 1000 V from a temperature-controlled aluminum chuck underneath an unlaminated sample stack to the top copper electrode placed on the stack. The stack was composed of soda-lime glass, an ethylene vinyl-acetate copolymer sheet, and a conventional p-type c-Si solar cell. The investigated solar cell exhibited a large degradation of the fill factor and slight degradation of the open-circuit voltage. These degradations were mainly caused by a reduction in the parallel resistance, which is the same degradation behavior as that reported previously. This indicates that the cell-level PID test well reproduces the typical degradation behavior. However, the leakage current in the unlaminated sample stack at a relatively low temperature exhibited a different temperature dependence from that in a laminated sample stack. The difference in the temperature dependence was caused by temperature-dependent contact resistances within the unlaminated sample stacks. This indicates that there is a difference between the temperature dependences in cell-level and module-level PID tests. This difference in the temperature dependence was reduced by the use of a heavier top electrode. These findings may assist in choosing the proper test conditions for this kind of cell-level PID test. A cell-level PID test for an n-type front-emitter c-Si solar cell was also performed. A typical degradation behavior, characterized by reductions in the open-circuit voltage and the short-circuit current, was observed, which implies that this test can be widely applied to PID phenomena occurring in many kinds of solar cells.

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1. Introduction

Potential-induced degradation (PID) has been identified as one of the most important reliability issues of photovoltaic (PV) modules deployed in large-scale PV systems (Luo et al., 2017). Relatively high electric-potential differences can exist between the frame and cells in PV modules deployed in such systems, which may lead to significant performance losses. This kind of degradation is called PID, and has been reported to occur in various types of PV modules, such as conventional p-type crystalline silicon (c-Si) (Hacke et al., 2010; Pingel et al., 2010; Berghold et al., 2010), front-emitter n-type c-Si (Hara et al., 2015, 2017; Yamaguchi et al., 2016a; Bae et al., 2017), rear-emitter n-type c-Si (Yamaguchi et al., 2016b, 2016c), n-type back-contact c-Si (Swanson et al., 2005; Naumann et al., 2014a), amorphous Si (a-Si) thin-film (Osterwald et al., 2003; Masuda and Hara, 2017), c-Si/a-Si heterojunction (Yamaguchi et al., 2017), cadmium telluride thin-film (Hacke et al., 2015, 2016a), and copper indium gallium selenide thin-film (Fjällström et al., 2013; Hacke et al., 2015; Yamaguchi et al., 2015) PV modules, and PV modules with different types of cells are known to degrade with different degradation mechanisms.

To investigate individual PID phenomena, several kinds of PID tests have been used (Luo et al., 2017). In particular, module-level PID tests have been considered basic methods to investigate the PID phenomena. These module-level PID tests have been successfully used to elucidate the influence of environmental factors, the effect of module components, kinetics of PID, and so forth. In such tests, it is, however, difficult to isolate the degraded solar cells and subject them to analyses, such as electron microscopy, because the module components strongly adhere to the cells. This has been a barrier to determining the root cause of PID.

To overcome the difficulty, a cell-level PID test was developed in the Fraunhofer Center for Silicon Photovoltaics (Lausch et al., 2014) and has been successfully used to elucidate the root cause

* Corresponding author.
E-mail address: s-yamaguchi@jaist.ac.jp (S. Yamaguchi).

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of PID. In this test, module-like layer stacks without lamination are used, which significantly reduces the effort to prepare samples, which enables a quick testing of the PID susceptibility of module components and cells. However, of most importance is the ease with which PID-affected bare cells can be obtained after PID tests, which enables investigation of the root cause in more detail. By using this test, the understanding of PID phenomena occurring in p-type c-Si PV cells has been improved (Naumann et al., 2013, 2014b, 2016). Despite the importance of the cell-level PID test, to date, the degradation behavior and the effects of the test conditions have not been discussed in detail. A comparison between the cell-level and module-level PID tests has not yet been made. These findings may help us select the proper test conditions for this kind of PID test.

In this study, we first investigated whether a typical degradation behavior can be reproduced in the cell-level PID test. We also clarified the effects of the test conditions, such as temperature and pressure applied to samples, on the degradation rate and the leakage current. On the basis of the obtained results, we will discuss the difference between the cell-level and module-level PID tests. In the cell-level PID test, the degradation rate was confirmed to positively correlate with temperature, which is similar to that observed in module-level PID tests; however, we observed that the dependence of the leakage current on temperature in the cell-level PID test was different from that in module-level PID tests. This modification is proposed to arise from the temperature dependence of interface contact resistances within the unlaminated sample stacks. The applied pressure, which is a specific parameter in the cell-level PID test, was found to reduce the difference in the temperature dependence.

2. Experimental procedure

Module-like stacks composed of 0.7-mm^2-thick flat soda-lime glass, a 0.4-mm-thick uncured ethylene vinyl-acetate copolymer (EVA) sheet, and a PID-prone p-type c-Si solar cell were prepared. The stacks were placed on a temperature-controlled aluminum (Al) chuck in a test chamber, with the cell side down, and a 0.05-, 0.10-, or 0.15-kg-weight copper block was placed on the glass. The copper blocks, the glass, and the EVA sheets had an area of 19.8×19.8 mm^2, whereas the solar cells had an area of 20×20 mm^2. This meant that there was no current flow through the edge surfaces of the solar cells. The copper block served as both the top electrode and a weight to reduce the contact resistance within the unlaminated sample stacks. The pressure applied to the sample stacks was changed by exchanging the copper block for another copper block with a different weight, where the pressures applied from the 0.05-, 0.10-, and 0.15-kg-weight copper blocks were 1.2, 2.5, and 3.7 kPa, respectively. The chamber was pumped with a diaphragm pump during the PID tests, which assisted in achieving good contacts between the components by eliminating air bubbles lying at the interfaces between the components. PID tests were performed by applying a voltage of 1000 V to the copper block with respect to the Al chuck maintained at 65 or 75 °C, using a PID Insulation Tester (KIKUSUI, TOS7210S) with an ammeter to detect the leakage currents during the voltage application. The voltage condition was the negative bias condition in the typical module-level PID tests. Leakage current densities were calculated by dividing the measured leakage currents by an area of 19.8×19.8 mm^2, which corresponded to those of the copper blocks, the glass, and the EVA sheets. Note that the front and rear electrodes of the solar cells were shorted in most of module-level PID tests whereas they were not shorted in this cell-level PID test. The diode of the investigated solar cells was therefore reverse-biased during the course of the PID tests. However, this was not a problem because the resistance of the encapsulation materials was considerably larger than that of the diode in the reverse-bias condition. We also used EVA sheets, which were cured in advance at 135 °C for 20 min in an electric furnace, to investigate the effects of the use of cured EVA sheets on the degradation rate.

After each PID test, the glass and the EVA sheet were carefully removed from the surface of the solar cell. To estimate the degradation, dark and one-sun-illuminated current density–voltage (J–V) and external quantum efficiency (EQE) measurements were taken on bare solar cells before and after the PID tests. These measurements were performed at 25 °C. Leakage currents were collected at elevated temperatures with a wider range from 55 to 85 °C under different test conditions to obtain the Arrhenius plots.

We also performed a PID test of a laminated stack composed of soda-lime glass, the EVA sheet, and the p-type solar cell in the same chamber by applying a voltage of 1000 V to the 0.05-kg-weight copper block placed on the cover glass with respect to the underlying Al chuck maintained at a temperature ranging from 55 to 85 °C. Additionally, the front and rear electrodes of the investigated solar cell were not shorted in this test. During the PID tests, the leakage current was determined. These data were compared with those from the cell-level PID tests. The sample stack had no rear EVA sheet or backsheet and was prepared using the same module encapsulation materials as those used in the cell-level PID tests. The module-lamination process was the same as that used in a previous study (Yamaguchi et al., 2016b). Because the sample stack experienced a standard module-lamination process, this test was considered as a kind of module-level PID test. We can therefore determine the differences between cell-level and module-level PID tests by comparing the results of this test with those of the cell-level PID tests.

We also performed the cell-level PID test in which an n-type front-emitter c-Si solar cell was stressed under a voltage of 1000 V, a pressure of 1.2 kPa, and a temperature of 65 °C, to further investigate whether the cell-level PID test can reproduce the typical degradation behavior.

3. Results and discussion

3.1. Degradation behavior of a PID-prone p-type c-Si solar cell

To investigate whether our PID test setup can reproduce the typical degradation behavior, we show the cell-level PID test result of the PID-prone p-type c-Si solar cell. Fig. 1 shows the one-sun-illuminated and dark J–V data before and after the cell-level PID test at a voltage of 1000 V and a pressure of 1.2 kPa at 65 °C. The fill factor (FF) and the open-circuit voltage (V_{oc}) decreased with increasing the PID-stress duration (Fig. 1a). From Fig. 1b, the decrease in the FF was mainly caused by a reduction in the parallel resistance. All the investigated samples with p-type c-Si solar cells showed a typical shunting behavior after the PID tests. This result demonstrates that this kind of cell-level PID test can, without lamination, reproduce the typical PID shunting behavior that has been frequently observed in both module-level PID tests and systems in operation.

3.2. Effects of temperature and applied pressure on the progression of PID

Fig. 2 shows the effect of temperature on the progression of the PID of the p-type c-Si solar cells in the cell-level PID test, where a voltage of 1000 V and a pressure of 1.2 kPa were applied. Obviously, the high temperature also accelerated the degradation rate in the cell-level PID tests. This temperature effect partially arose from a temperature-activated ion drift within the sample stack.

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