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Multi-wire metallization for solar cells: Contact resistivity of the interface between the wires and In_2O_3:Sn, In_2O_3:F, and ZnO:Al layers

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ABSTRACT

Replacing expensive silver with inexpensive copper for the metallization of silicon wafer solar cells can lead to substantial reductions in material costs associated with cell production. A promising approach is the use of multi-wire design. This technology uses many wires in the place of busbars, and the copper wires are "soldered" during the low-temperature lamination process to the fingers (printed or plated) or to the transparent conductive oxide (TCO) layer, e.g. in the case of the α-Si/c-Si heterojunction cells. We have studied the effects of Si surface morphology (textured or planar) and TCO resistivity (ρ) on the contact resistivity (ρ_C) between wires and TCO (In_2O_3:Sn (ITO), In_2O_3:F (IFO), and ZnO:Al (AZO)) layers grown on silicon substrates by ultrasonic spray pyrolysis. To determine ρ_C by transmission line model (TLM) measurements, we have developed a specialized TLM test structure which takes into account specifics of laminated contacts. It has been shown that, if the longitudinal resistance of the wires is left out of account, the error in ρ_C determined by TLM measurements may reach tens or hundreds of percent or even more. To eliminate such errors, we have adjusted the TLM measurement procedure. The present results demonstrate the following: (i) In all the groups of our samples, ρ_C increases with ρ and the $\rho_C(\rho)$ data can be represented by a power-law trend line. (ii) For ITO and IFO, ρ_C is lower in the case of a textured surface: 0.3–6 mΩ cm^2 at ρ = 0.2–3 mΩ cm. (iii) In contrast, for the AZO films ρ_C is lower in the case of a planar Si surface: 5–140 mΩ cm^2 at ρ = 9–80 mΩ cm. These findings have been used to analyze the series resistance (R_s) of AZO/n-Si heterojunction solar cells. The contribution of ρ_C to R_s has been shown to reach 30–40%.

1. Introduction

Metallization is a process step that has a direct substantial impact on the efficiency and the cost of solar cells. For diffused-junction wafer-based crystalline silicon (c-Si) solar cells, which currently dominate in the industry, high temperature (800–900 °C) screen printing of metal pastes (silver and aluminium containing pastes) are used to form metallic electrodes (Goodrich et al., 2013). However, high-temperature screen printing is not suitable for solar cells with transparent conductive oxide (TCO) layers, which are used as an antireflection coating (ARC) and as a transparent electrode for charge carrier collection. It should be noted that TCO layers are an almost unavoidable component in most types of solar cells, first and foremost in the organic, dye sensitized, perovskite, and thin-film solar cells (based on CdTe and Cu(In,Ga)Se_2 compound semiconductors, amorphous (α-Si:H) and microcrystalline silicon) (Liu et al., 2010; Razykov et al., 2011), and also in various kinds of c-Si solar cells based on the α-Si/c-Si heterojunction (Ballif et al., 2014; Barraud et al., 2013), TCO/c-Si heterojunction (Bivour et al., 2015; Gerling et al., 2016; Pietruszka et al., 2016), and diffused p–n junction (Feng et al., 2015; Kim et al., 2013; Khan et al., 2013; Le et al., 2014).

For c-Si solar cells with TCO layers, the metallic grid at the front side is usually also formed by screen printing of Ag pastes followed by sintering (Ballif et al., 2014; Barraud et al., 2013; Feng et al., 2015; Kim et al., 2013; Khan et al., 2013; Le et al., 2014; Serenelli et al., 2014), however, at substantially lower temperatures (typically <200–250 °C), since annealing may significantly deteriorate the properties of the layers under the TCO, for example, the a-Si layers in α-Si:H/c-Si heterojunction solar cells and organic transport layers in organic solar cells. In addition, annealing can also affect the properties of the TCO electrodes (Ma et al., 2014; Serenelli et al., 2014), and also the properties of the metal/TCO (Barraud et al., 2013) and TCO/Si interfaces (Untila et al., 2013a). However, low-temperature pastes are more resistive than traditional high-temperature fired Ag pastes used for c-Si homojunction cells (Ballif et al., 2014; Serenelli et al., 2014). The higher resistivity

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of low-temperature pastes can be managed by depositing a larger amount of paste per cell, but this will also undesirably increase Ag consumption.

It should be emphasized that Ag pastes are expensive materials (next to Si wafers) in the manufacture of solar cells. Therefore, mainly because of the high price of silver, which is becoming increasingly incompatible with cost-effective photovoltaics, and, in addition, since just the limitation of Ag resources will, in future, be an obstacle for terawatt-scale deployment of c-Si photovoltaics (Tao et al., 2011), silver-free contact metallization is a topic of increasing interest for solar cell processing. Thus, substituting Ag with copper (Cu) metallization is a particularly relevant research topic as this would significantly lower the material costs associated with cell production.

Various approaches have been proposed for reducing silver consumption, in particular (i) the use of copper pastes instead of silver pastes (Yoshida et al., 2012); (ii) plating of a nickel–copper stack (Hernandez et al., 2013); (iii) the multi-wire approach, which uses many solder-coated wires instead of a few (usually three) busbars, and the wires are "soldered" to printed or electroplated fingers in the lamination process (the multi-wire approach allows silver consumption to be reduced owing to the less stringent requirements for the longitudinal resistance of the fingers) (Papet et al., 2015); and finally (iv) an approach in which a current-collecting grid consists of only an array of solder-coated wires, which are attached to a TCO layer by lamination film and form direct contact to the TCO without any printed or electroplated fingers.

The last approach was implemented by our group as a laminated grid cell (LGCell) design, schematized in Fig. 1. Laminated wires were used to make contacts to various TCO layers: In_2O_3:Sn, In_2O_3:F, ZnO:Al, and ZnO:Ga. Using Czochralski silicon (Cz-Si) wafers, we produced TCO/Si heterojunction solar cells of the LGCell design (in particular, those with IFO/(pp$^+$)Cz-Si/ITO (Untila et al., 2013a) and AZO/(nn$^+$)Cz-Si/IFO (Untila et al., 2016) structures) and bifacial low-concentration p–n junction c-Si solar cells: IFO/(n$^+$pp$^+$)Cz-Si/ITO (Untila et al., 2014), ITO/(p$^+$nn$^+$)Cz-Si/IFO (Untila et al., 2012a), and GZO/(p$^+$nn$^+$)Cz-Si/IFO (Untila et al., 2015a).

Note in passing that it is a mistaken belief that the multi-wire approach was "initially developed by Day4Energy and commercialized under the name SmartWire" (Ballif et al., 2014). For the sake of fairness, it should be mentioned that actually the concept of a current-collecting grid based on wire contacts was first proposed by our research group (MSU) (Rubin et al., 1992). New ideas proposed by our group in subsequent work ensured significant advances in developing the concept. One such idea was to fabricate a so-called "workpiece," i.e. an intermediate "product" that had the form of an array of wires pressed into a thin adhesive layer of lamination film. Samples of such elements were tested at the Sandia National Laboratories as early as 2000 (Untila et al., 2001). Well afterward, in 2004, the idea was patented under the name Day4™ Electrode by Day4 Energy, a company founded by former members of our laboratory (Rubin and Rubin, 2004). It is important to note that we used such workpieces to make contacts not only to TCO layers but also to printed contacts: to a backside Al layer and Ag fingers on the frontside of solar cells.

A key metallization parameter is contact resistivity (ρ_C), which contributes to the series resistance (R_s) of the solar cell and, accordingly, influences its efficiency. However, the contact resistivity between TCO layers and laminated soldered wires has not yet been studied in sufficient detail.

In this paper, we present ρ_C data for contacts between laminated wires and ITO, IFO, and AZO layers grown on silicon by ultrasonic spray pyrolysis (USP). In addition, we examine how ρ_C is influenced by the surface morphology of the silicon (textured or planar) and the resistivity of the TCO. We studied TCO layers similar to those used previously in producing solar cells.

To determine the ρ_C of contacts between laminated wires and TCO layers, we had to adjust the transmission line model (TLM) measurement procedure, which is typically used to determine ρ_C (Reeves and Harrison, 1982). The point is that laminated wire contacts are coated with lamination film, which prevents electrical contact between measuring needle probes and the wire in the region where it is in contact with the TCO. Because of this, specially designed contact pads located some distance from the sample should be used in TLM measurements (Fig. 2). Analysis carried out in this study suggests that, in such a case, with the longitudinal resistance of the wires (situated both outside and on the test structure) left out of consideration, standard TLM measurements yield ρ_C with a considerable error, which reaches tens or hundreds of percent or even more in many cases of practical importance. The adjusted measurement procedure described in this report eliminates such errors. Note that similar test structures in which contact to thin, long metallic strips is made outside the sample are encountered in the literature (Peng et al., 2015), but the effect of the longitudinal contact resistance has not been assessed. In this study, the experimental ρ_C data are used to analyze the series resistance of AZO/n-Si heterojunction solar cells.

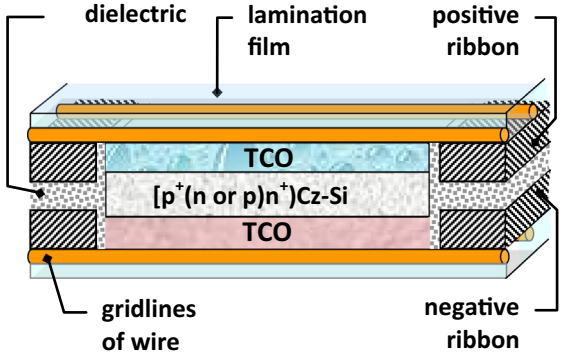

Fig. 1. Schematic diagram of a bifacial LGCell silicon solar cell with TCO/[p$^+$(n or p)n$^+$]Cz-Si/TCO structure.

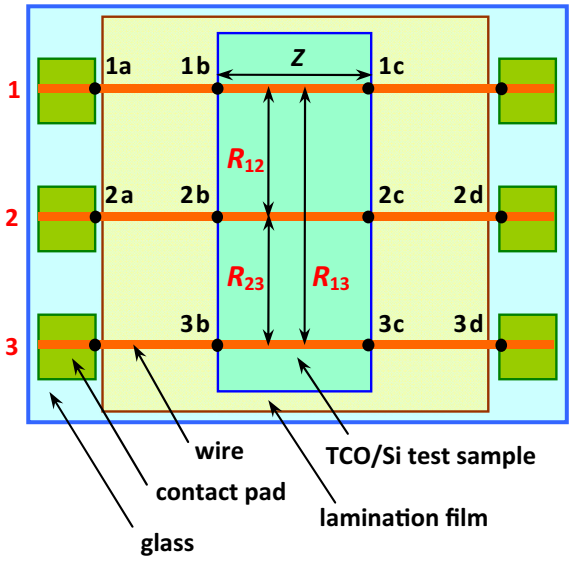

Fig. 2. TLM test structure used to measure the contact resistance R_C between the TCO layer and laminated wires. See text for details.