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Spacer defined FinFET: Active area patterning of sub-20 nm fins with high density

B. Degroote, R. Rooyackers *, T. Vandeweyer, N. Collaert, W. Boullart, E. Kunnen, D. Shamiryan, J. Wouters, J. Van Puymbroeck, A. Dixit, M. Jurczak

IMEC vzw, SPDT, Kapeldreef 75, B-3001 Leuven, Belgium

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Abstract

We present a method to obtain Si-fins with a critical dimension (CD) below 20 nm, separated by a minimum distance of 25 nm and connected by a common source/drain (S/D) pad. The method comprises of recursive spacer defined patterning to quadruple the line density of a 350 nm pitch resist pattern defined by 193 nm lithography. Spacer defined patterning is combined with resist based patterning to simultaneously define fins and S/D pads in a Silicon on Insulator (SOI) film. CD and Line Width Roughness (LWR) analysis was done on top down SEM images taken in a center die and in an edge die of a 200 mm wafer. The average CD is 17 nm in the center of the wafer and 18 nm at the edge. The LWR is 3 nm for both center and edge. Additional process steps to remove etch damage and round the top corner of the fin (i.e. oxidation followed by H_2 anneal) further reduce the CD to 13 nm.
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1. Introduction

FinFET devices currently receive a lot of attention because of their potential use in advanced nodes like the 32 nm-node and below. An important advantage over the planar architecture is the better control on Short Channel Effects (SCE) [1,2]. In addition, the FinFET architecture looks more promising for scaling [3]. The effective device width can be increased by increasing either the fin height or the fin density. The former option makes process integration more critical because of the increased topography. The latter is more demanding from lithographic point of view. Spacer patterning technology is very attractive in order to overcome the limits of conventional lithography techniques in terms of pattern density [4]. It enables to improve pattern fidelity and CD uniformity.

To our knowledge no reports have been made on spacer defined fins with a small CD (i.e. <20 nm) being successfully integrated in a MuGFET transistor. Choi et al. have demonstrated spacer defined Si-structures with sub-10 nm fins connected by source/drain pads [5]. However, for these structures no sacrificial oxidation step was done. This means that the etch damage is not removed. The authors of Ref. [5] further report on other fin structures where a thermal oxidation of 10 nm was done to remove the etch damage. However, these fins do not have a sub-20 nm CD (i.e. 20–25 nm) and additionally they do not have a straight profile. A relatively large oxide layer of 10 nm needs to be removed after oxidation, which results in a considerable recess of the Buried Oxide (BOX) and a large undercut of the fin and the S/D pad. No electrical results are reported for these fins. The same authors report only in Ref. [6] on the demonstration of a functional double-gate FinFET device with a 40 nm spacer defined Si-fin structure connected by S/D pads.

In this paper we present a method to obtain sub-20 nm fins, with a straight profile, separated by a minimum dis-

* Corresponding author.
E-mail address: rita.rooyackers@imec.be (R. Rooyackers).

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tance of 35 nm, and connected by a common S/D pad. This was achieved by two repetitions of spacer definition starting from a pattern with a pitch of 350 nm. The principle of recursively applying spacer defined patterning was demonstrated in Ref. [7]. Si-structures with a line width of 70 nm spaced by 80 nm were obtained from a conventional lithography pattern with a pitch of 600 nm after three repetitions of spacer definition. We have used the same principle but with a different integration scheme, obtaining a considerably smaller fin CD with a considerably smaller separation. In addition, the fin structures presented in this paper can be successfully integrated for logic applications by using an extra mask to clear out part of the spacer hard mask in areas were only one fin is needed. Thus an extra mask is required if single fins with the same dimension are needed. Wider fin regions can be defined together with the common S/D pads, thus by conventional lithography.

2. Experiment

The experiments related to optimizing the necessary process steps have been done on 200 mm bulk Si-wafers and dummy silicon on insulator (SOI) substrates. A dummy SOI wafer consists of 65 nm RTCVD amorphous Silicon (a-Si) deposited on top of 150 nm thermal oxide. For the Line Width Roughness (LWR) study real SOI wafers (UNIBOND) have been used with 70 nm p-type Si(1 0 0) on top of 145 nm buried oxide (BOX). The process flow to apply recursive spacer defined patterning for the fin definition combined with resist based patterning for the S/D pad definition consists of a number of deposition, removal and lithography steps. In Table 1 we give an overview of the different tools that were used to grow, deposit and remove the layers involved.

The sacrificial SiGe hard mask and the S/D pad definition were done with 193 nm lithography using 77 nm ARC29A bottom anti-reflective coating (BARC) from Brewer Science/Nissan Chemical and 230 nm AR237J resist from JSR. For the definition of the alignment markers, I-line lithography was used with OIR620 from FFEM.

3. Results and discussion

In Section 3.1 we explain what process steps are needed to obtain high density fin patterning by recursive spacer defined patterning combined with the definition of S/D pads. In Section 3.2 we focus on the CD performance and the line width roughness analysis. In Section 3.3 some process issues are discussed.

3.1. Process flow

Before looking at some of the process steps individually we give an overview of the overall process flow, schematically shown in Fig. 1. First we pattern a sacrificial SiGe hard mask (HM) stopping on a thermal oxide layer grown on the SOI layer. Then we define the first spacer, which consists of RTCVD nitride (Fig. 1a). Subsequently the alignment markers are defined. In the next stage of the process flow the sacrificial SiGe pattern is removed in a mixture of ammonia with hydrogen peroxide (APM: 1:1:5 NH_4OH:H_2O_2:H_2O at 65 °C) (Fig. 1b). Subsequently a Tetraethyl Orthosilicate (TEOS) oxide layer is deposited (Fig. 1c) out of which the second spacer is defined next to the first spacer. The TEOS oxide spacer serves as the final HM for the patterning of the Si-fins. After that, the first (nitride) spacer is removed by dry etch (Fig. 1d). In the next step, the S/D pads are defined by 193 nm lithography (Fig. 1e). Then the SOI layer is patterned using the TEOS spacers as HM for the fins and the resist pattern as a mask for the S/D-pads (Fig. 1f). Finally, the resist is stripped and the oxide HM removed in HF, which results in a limited amount of BOX recess (Fig. 1g).

The classical approach for active area definition is to define the fins together with the S/D pads in one lithography step. We have decided to use the same structures to demonstrate the feasibility of recursive spacer defined patterning combined with resist based S/D definition. As such, we can easily compare the device performance for both approaches since the subsequent process steps (e.g. for gate definition, implantations, contact definition) are similar. In addition, we only need one extra reticle compared to the

Table 1
Overview of the different tools used to grow, deposit and remove the layers involved in the process flow

Functionality	Details	Tool
Growth	4 nm thermal oxide on surface of SOI wafer	A400 Furnace, ASM
Deposition	RTCVD of 60 nm $Si_{0.5}Ge_{0.5}$	Centura Platform, Applied Materials
	PECVD of 40 nm oxide	Centura Platform, Applied Materials
	RTCVD of 40 nm SiN	Centura Platform, Applied Materials
	LPCVD of 30 nm Tetraethyl Orthosilicate (TEOS) oxide	A400 Furnace, ASM
Plasma etching	Dual frequency planar triode system: dark field etch for alignment marker definition	Lam Exelan
	Inductively coupled plasma system: SiGe patterning, SiN spacer etch and removal, TEOS spacer etch and SOI patterning	Lam Versys2300

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