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A simple method for sub-100 nm pattern generation with I-line double-patterning technique

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ABSTRACT

We have developed a simple method adopting double-patterning technique to extend the I-line stepper limit for the sub-100 nm poly-Si pattern generation in this work. Through in-line and cross-sectional scanned electron microscopic analyses of the generated patterns, we confirmed the feasibility of the double-patterning technique for the fabrication of nano-scale devices. Resolution capability of this technique has been confirmed to be at least 100 nm, which is much superior to the resolution limit of conventional I-line lithography. This approach has also been applied for fabricating p-channel metal–oxide-semiconductor field-effect transistors. Excellent device characteristics were verified.

1. Introduction

The well-known Moore's Law states that the number of transistors on an integrated circuit (IC) chip will double every 18 months [1]. Since the advent of IC manufacturing, this law has been in force for decades. In order to keep up with the Moore's Law, shrinkage in device dimensions is indispensable, which also promotes device density, operation speed, and chip functionality. In other words, for better performance and cheaper manufacturing cost, the continuous scaling of the devices is evitable. To keep pace with the law, it requires innovation to overcome several fundamental physical barriers lying ahead, and first of all is to extend the photolithography limit. According to the Rayleigh's criterion, the resolution, R, of a photolithography technique can be expressed as follows [2]:

$$R = k_1 \lambda / NA, \tag{1}$$

where k_1 is a system constant, λ is the wavelength of incident light, and NA is the numerical aperture of the lithography system. Based on such criterion, we could adjust the three factors of the criterion so as to boost the resolution of a lithography system [3–5]. Nowadays, state-of-the-art mass production of nano-scale ICs employs the immersion lithography tools with the 193 nm excimer laser as the exposure light source, which has been widely adopted in 300-mm wafer fabrication for manufacturing chips with sub-100 nm technology node. However, the extremely high cost on the lithography tool and related processes hinders these tools from being used in the laboratories of universities. On the other hand, electron-beam lithography [5] is therefore far more popular in these environments for generating sub-100 nm patterns, although the throughput is dramatically limited, and thus its proliferation in mass manufacturing is prohibited.

Recently, it was reported that the double exposure (DE) technique [6], and double-patterning (DP) technique [7–9] were being considered as promising candidates to extend lithography processing beyond the 45 nm node at k_1 factors below 0.30. DP is a process that splits one patterning step into two to relax the imaging fidelity requirements for small technology nodes. The most common form of DP typically decomposes a target layout pattern into two separate photomasks employing two exposure steps and subsequent etching steps. Consequently, the dimensions of the final target patterns can easily break the resolution limit with single exposure. Usually I-line stepper is not capable of sub-100 nm pattern generation owing to its long exposure wavelength of 365 nm. In this work, we develop a DP technique with conventional I-line stepper to generate sub-100 nm photoresist (PR) patterns with the goal to fabricate nano-scale MOSFETs. Although this technique consists of two times the lithographic and subsequent etching steps, we show that the DP method could reliably generate line patterns with dimension down below 100 nm. Our results indicate that the method developed in this work is promising for both the research works carried out at universities and for practical manufacturing in terms of much lower cost (as compared with state-of-the-art DUV lithography) and decent throughput.

2. Experiments

For all lithographic steps carried out in this work, we used an I-line stepper (Canon FPA-3000i5+) to generate the photoresist (PR)

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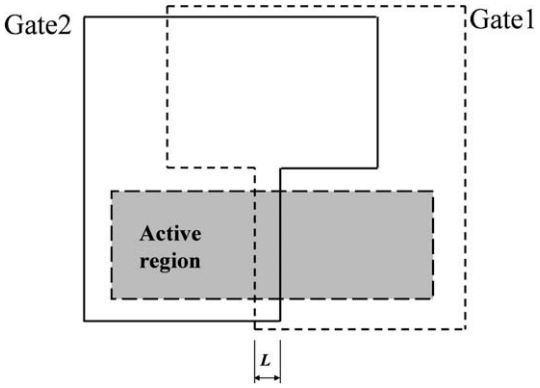

Fig. 1. Mask layouts for defining the gate pattern on the active region. Gates 1 and 2 represent the two masks used in the DP process. Channel length of the device is determined by the overlap region of the two masks in the active region.

patterns. We have implemented the DP technique on the practical fabrication of nano-scale p-channel metal–oxide-semiconductor field-effect transistors (pMOSFETs). Fig. 1 is the schematic of the two masks used for generating the gate patterns. The most critical portion in the design is the overlapped region of the two gate patterns in the active area which determines the channel length (L) of the fabricated device.

Fig. 2 illustrates the major process steps in the device fabrication. Local oxidation of Si (LOCOS) scheme was first used for device isolation. N well was then formed by P^+ implantation with energy of 120 keV and dose of $7.5 \times 10^{12}\ cm^{-2}$, followed by an anneal at 1100 °C for dopant drive-in. Next, channel stop implantation was performed by implanting As^+ (120 keV, $3 \times 10^{12}\ cm^{-2}$), followed by wet oxidation to form 550 nm-thick field oxide. Anti-punch through and threshold voltage adjustment implantations were performed individually by implanting P^+ (120 keV, $4 \times 10^{12}\ cm^{-2}$) and As^+ (80 keV, $1 \times 10^{13}\ cm^{-2}$), respectively. Thermal gate oxide of

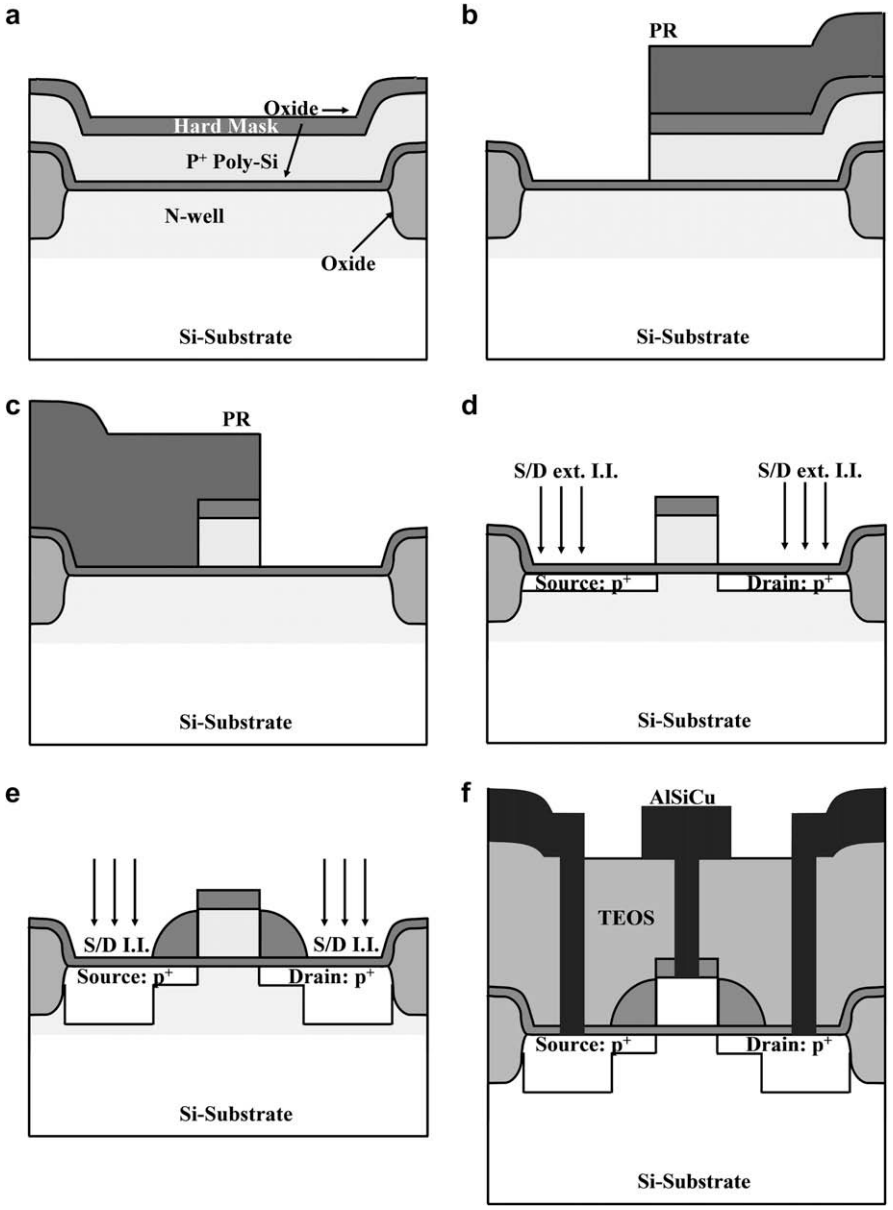

Fig. 2. Process flow of a pMOSFET with the DP method. (a) Deposition of TEOS and poly-Si layers onto the gate oxide (active region) and field oxide (isolation region). (b) First gate pattern definition. (c) Second gate pattern definition. (d) S/D extension implantation. (e) Spacer formation and deep S/D implantation. (f) Formation of contact holes and test pads.