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A 0.35 μm CMOS divide-by-2 quadrature injection-locked frequency divider based on voltage–current feedback topology

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ABSTRACT

This paper presents a new divide-by-2 quadrature injection-locked frequency divider (QILFD). The QILFD consists of a new transformer-coupled quadrature voltage controlled oscillator (QVCO) with the voltage–current feedback technique and two NMOS switches, which are in parallel with the QVCO resonators for signal injection. The proposed CMOS QILFD has been implemented with the TSMC 0.35 μm CMOS technology and the core power consumption is 16.52 mW at the supply voltage of 2.2 V. The free-running frequency of the QILFD is tunable from 2.85 GHz to 3.07 GHz. At the input power of 0 dBm, the divide-by-2 operation range is from 5.48 GHz to 6.48 GHz. The phase deviation of free running quadrature output is about 0.53°.

1. Introduction

Recently, the direct conversion transceiver architecture has been widely used because of the feasibility of low power and low cost single-chip transceivers, in which quadrature oscillators play a key role. Quadrature injection-locked frequency dividers (QILFDs) provide quadrature-phase outputs and can be used with a master VCO to form a frequency plan in direct-conversion transceivers. The main advantage of using QILFDs generate the quadrature signals, which is breaking the tradeoff between spectral purity and phase accuracy, the major limit of coupled VCOs [1]. QILFD can be formed by two independent divide-by-2 ILFDs [2,3] with a single-ended injection MOSFET. The phase accuracy depends upon the accuracy of the differential injection signals from the master VCO. QILFD also can be formed by injecting a differential signal to the two injection MOSFETs in a quadrature VCO (QVCO) as shown in Fig. 1 [4,5].

The QILFDs in the literature have been implemented in advanced CMOS technology [2,3]. In this paper, a new divide-by-2 LC tank QILFD is proposed, and it was implemented in the 0.35 μm CMOS technology. The 0.35 μm CMOS technology has been widely adopted to design a low cost product, and only a few divide-by-2 ILFDs with differential outputs [6,7] have appeared in literature recently. The existing 0.35 μm QILFD [8] uses two levels of transistors and consumes larger power. A quadrature ILFD can consume much lower power than a conventional logic divider and it can work adequately with a low-level VCO input and generates an output with a sufficient signal level to properly drive the next stage. The proposed transformer-coupled QILFD is based on a new quadrature VCO using the voltage–current feedback technique, and it consumes lower power than the QILFD in [8].

This paper is organized as follows. Section 2 describes the operation principle of the proposed QILFD circuit and the circuit constituent components. Section 3 describes the experimental results, and Section 4 is a conclusion.

2. Circuit design

Fig. 2a shows the schematic of the proposed divide-by-2 QILFD, which consists of a new quadrature VCO with two direct injection MOSFETs (M9, M10). The circuit can operate as a divide-by-2 frequency divider by applying an external differential injection signal to the gates of transistors (M9, M10) with a dc gate bias Vinj. The QILFD consists of two identical half-circuits, which cannot oscillate alone. The cross-coupled transistors (M1–M4) contribute an effective negative resistance to compensate for the tank loss. Two resonators respectively consist of L5, L6, Cv and L7, L8, Cv, which are embedded in each half circuit. The NMOSFETs (M5–M8) are dc biased at Vb. Vtune is the tuning voltage and Cv is NMOSFET varactor used for frequency tuning. Varactors connected in back-to-back are used for frequency tuning. The two half-circuits are coupled by the transformer coupling technique to form the QVCO and the QILFD. The transformers (L3, L6 and L4, L5) feedback the output voltages in the second half-circuit to the inputs in the first half-circuit. And the transformers (L1, L7 and L2, L8) feedback the output voltages in the first half-circuit to the inputs in the second half-circuit. The transconductors M5–M8 convert voltage to current and the voltage-to-current feedback ensures that the complete circuit can oscillate as a QILFD.

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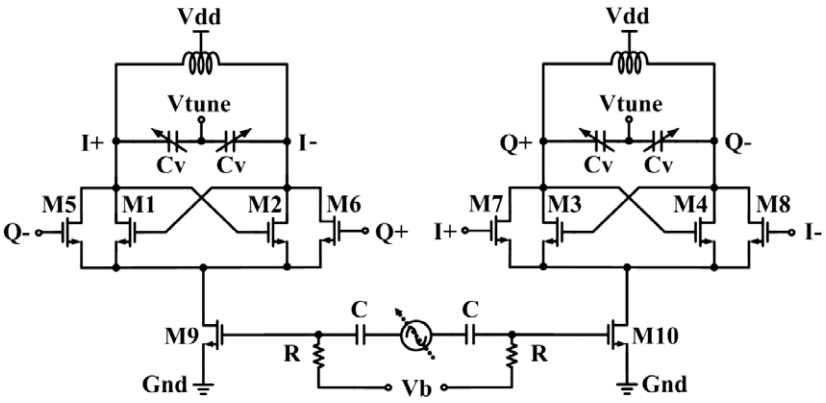

Fig. 1. Schematic of the conventional QILFD.

Fig. 2b shows the equivalent block diagram of the proposed QILFD and m is the transconductance coupling coefficient. In Fig. 2b, g_{Mi} ($i = 1–4$) is the transconductance of Mi, the ac voltages at the QILFD cores outputs are respectively denoted as X_A, X_B, X_C and X_D, the gate voltage X_A of M2 is approximately equal to $(mX_C + g_{M1}X_B)Z_L$, where the current mX_C is generated by M5 and is coupled by the transformer (L4 and L5) from node C, and Z_L is the net resonator load impedance. The ac voltage X_A can be expressed as:

$$X_A = (mX_C + g_{M1}X_B)Z_L \tag{1}$$

Because of $X_A = -X_B$, (1) can be modified as:

$$X_A = (mX_C - g_{M1}X_A)Z_L \tag{2}$$

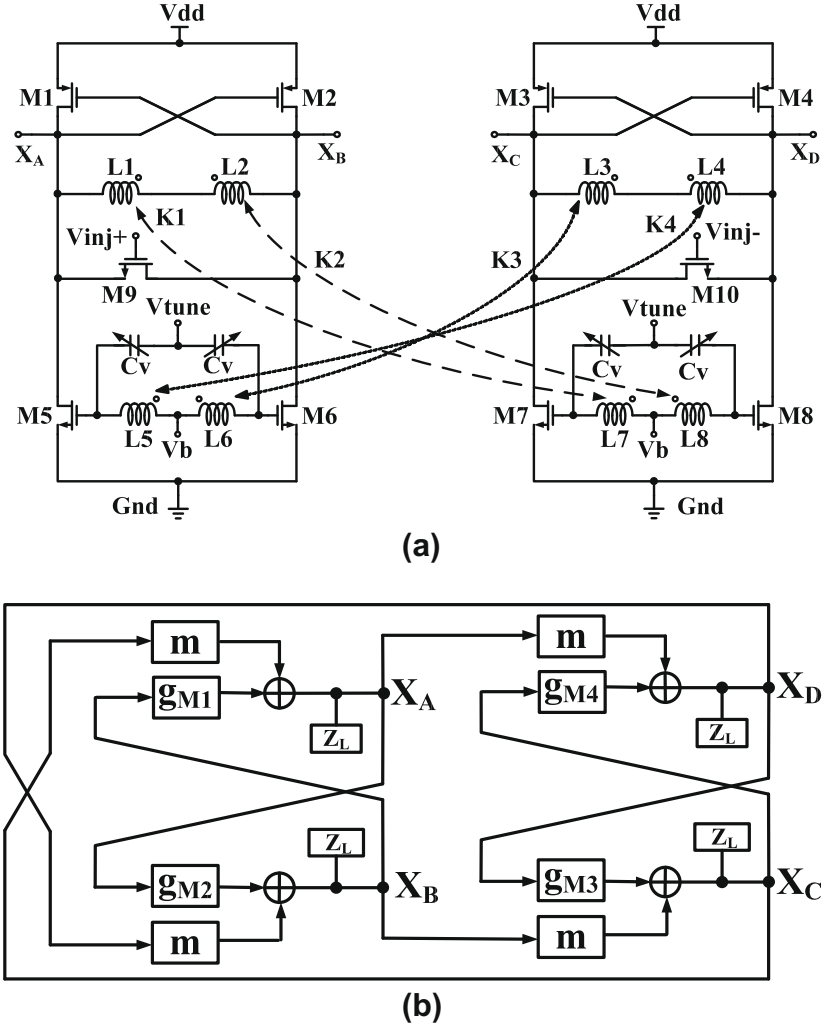

Fig. 2. (a) Proposed QILFD and (b) simplified equivalent block diagram.