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Statistical variability in FinFET devices with intrinsic parameter fluctuations

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ABSTRACT

High-κ/metal-gate and vertical channel transistors are well-known solutions to continue the device scaling. This work extensively estimates the influences of the intrinsic parameter fluctuations on nanoscale fin-type field-effect-transistors and circuits by using an experimentally validated three-dimensional device and coupled device-circuit simulations. The dominance fluctuation source in threshold voltage, gate capacitance, cut-off frequency, delay time, and power has been found. The emerging fluctuation source, workfunction fluctuation, shows significant impacts on DC characteristics; however, can be ignored in AC characteristics due to the screening effect of the inversion layer.

1. Introduction

In nano-device-circuits and systems, the device variability is pronounced and becomes crucial for circuit design [1–9]. The most well-known fluctuation sources on transistors are the random-dopant-fluctuation (RDF) and process-variation-effect (PVE) [4,6,7]. The RDF comes from the manufacturing process, such as ion implantation, thermal annealing and so on. Fluctuations of device characteristics including are caused both by a fluctuation in the number of dopants and the particular random distribution of dopants in the channel region [7]. The inevitable variations of processing conditions, such as the resolution limit of lithography and the grainy nature of photo resist and gate, also impact the device dimensions. The gate length deviation and the line edge roughness are the dominating factors in PVE [4,6,7]. To suppress the impact of these variations, fin-type field-effect-transistors (FinFETs) [10–12] and high-κ/metal-gate technology [13] are promising. However, the use of metal as gate material may introduce another source of fluctuation, workfunction fluctuation (WKF). The grain orientation of metal is uncontrollable during growth period [14]; therefore, the device threshold voltage (V_{th}) will become a probabilistic distribution rather than a deterministic value. Approach has been noticed the workfunction fluctuation (WKF); unfortunately, only the device V_{th} fluctuation was concerned and the scope is limited to the planar transistors [14,15].

In studying the fluctuation of FinFETs, diverse approaches have recently been presented [10–12]; however, the attention is most drawn to the existence of RDF and PVE on transistors. A comprehensive understanding of these fluctuations including WKF on FinFETs and circuits is lacked. Therefore, this study explores the intrinsic device parameter fluctuations (WKF, PVE, and RDF) on 16-nm-gate silicon-on-insulator (SOI) FinFETs and digital circuits by an experimentally validated three-dimensional coupled device-circuit simulation technique [8,9]. The major variability sources in device's DC/AC and circuit's timing/power characteristics are explored for the first time. The vast study assesses the fluctuation on digital circuit performance and reliability, which can be in turn used to optimize nanoscale devices and circuits.

2. Simulation technique

Fig. 1a illustrates the explored 16-nm-gate SOI FinFETs with amorphous-based TiN/HfSiON gate stacks with an EOT of 1.2 nm [14]. The equivalent channel doping concentration is $1.48 \times 10^{18}\,cm^{-3}$. Fig. 1b–d illustrates the RDF-induced fluctuation, the simulation mainly follows our recent work [7–9]. The PVE-induced fluctuation is examined by V_{th} roll-off characteristics, as shown in Fig. 1e [7]. The physical models and accuracy of such large-scale simulation approach have been quantitatively calibrated by experimentally measured results [7,10]. For WKF in Fig. 1f, a Monte-Carlo approach is proposed for examining such effect, as shown in Fig. 1g. Based on the average grain size, 4 nm [14,15], the gate area is first partitioned into several parts. Then, the workfunction of each partitioned area (WK_i) is randomized following the properties of metal in Fig. 1h [14,15]. The effective device workfunction is then obtained and used for estimation of WKF-induced fluctuations. Fig. 1i is the explored inverter circuit, in which a coupled device-circuit simulation approach [8,9] is employed to ensure the best accuracy. Notably, the device dimension and V_{th} of both *n*-type and *p*-type transistors are the same to compare them on the same basis.

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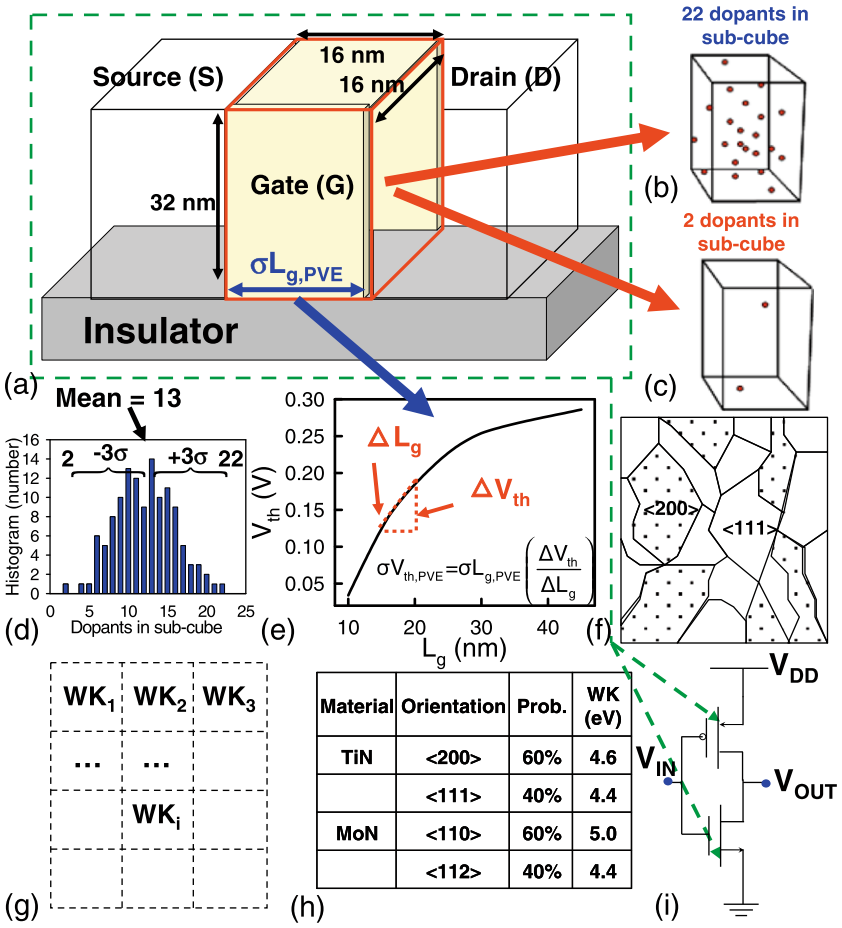

Fig. 1. (a) The explore SOI FinFET with RDF effect. The number of channel dopants in device may vary from 2 to 22, and the average number is 13(b–d). (e) The V_{th} roll-off characteristics for estimating PVE. (f) Metal-gate surface morphology. (g) In estimation of WKF, the gate area is partitioned into several pieces according to the average grain size. The workfunction of each partitioned area (WK_i) is a random value, whose probability follows (h). (i) The tested inverter circuit.

3. Results and discussion

Fig. 2a and b displays the components of σV_{th} for *n*-type and *p*-type planar MOSFETs and FinFETs, respectively. The total σV_{th}, $\sigma V_{th,total}$, are obtained from the statistical addition as shown in below:

$$(\sigma V_{th,total})^2 - (\sigma V_{th,PVE})^2 + (\sigma V_{th,WKF})^2 + (\sigma V_{th,RDF})^2 \quad (1)$$

The σVth,PVE, σVth,WKF, and σVth,RDF are the PVE-, WKF-, and RDF-induced σVth, respectively. The FinFET shows a significantly smaller σVth than the planar MOSFET due to its better channel controllability [10]. The RDF and WKF dominate the σVth in both n-type and p-type transistors. The σVth,WKF in p-type FinFETs becomes comparable to σVth,RDF due to the large deviation of workfunction. In Fig. 1h, the probability for the used material TiN (for NMOS) and MoN (for PMOS) are the same; however, the differences of workfunction in different grain orientation are quite different. The large deviation of workfunction in MoN enlarges the σVth,WKF of p-type FinFETs and makes the σVth,total of p-type FinFETs larger than the n-type FinFETs. Notably, the simulation result is still valid for lightly-doped transistors, in which the lightly-doped channel is employed for the suppression of RDF. With similar simulation methodology, the WKF possesses over 95% Vth fluctuation of σVth,total, which shows the significance of controlling WKF. Fig. 3 summarizes the gate capacitance fluctuations (σCg) with 0 V, 0.5 V and 1.0 V gate bias. Different to the results of Vth fluctuation, the WKF brought less impact on gate capacitance fluctuation. At low gate bias or negative gate bias, the accumulation layer screens the impact of WKF. Additionally, at low gate bias, the total capacitance decreases because of an increased depletion

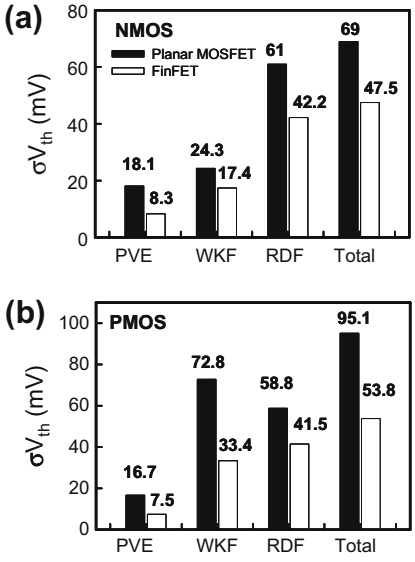

Fig. 2. The components of σV_{th} for (a) *n*-type and (b) *p*-type planar MSOFETs and SOI FinFETs.