Microelectronics Reliability 49 (2009) 977–981

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

CMOS logic gate performance variability related to transistor network arrangements

Digeorgia N. da Silva *, André I. Reis, Renato P. Ribas

PPGMicroelectronics – Federal University of Rio Grande do Sul, Av. Bento Gonçalves 9500, CEP 91501-970, Porto Alegre, RS, Brazil

ARTICLE INFO

Article history:
Received 29 June 2009
Available online 12 August 2009

ABSTRACT

The rapid scaling of CMOS technology has resulted in drastic variations of process parameters. Since different transistor arrangements present different electrical characteristics, this work analyzes the impact of process variability in performance of logic gates, according to their topology and the relative position of the switching device in the network. Results have been obtained through Monte-Carlo simulations and design guidelines for parametric yield improvement have been derived.

1. Introduction

Manufacturing variations may lead to significant discrepancies between designed and fabricated integrated circuits. Due to the shrinking of device size, the relative impact of critical dimension variations tends to increase at each new technology generation, since the process tolerances do not scale at the same rate [1]. Many studies about effects of intrinsic processes variations on the functionality and reliability of circuits have been done in recent years [2–6]. Since process variations become a more critical issue due to aggressive technology scaling, the migration from deterministic to statistical analysis of circuit designs may reduce conservatism and failure risk compared with applying the traditional worst-case corner approach. The traditional corner-case static timing analysis (STA) technique seems as a reasonable way to handle global variations on a wafer but not local ones [7,8]. In terms of circuit performance, a logic gate may become slower for a certain variation and faster for another, and that might depend on its location on a die. The importance of intra-die variations has grown as well, and the number of process parameters which present considerable variations has also increased. Such situation requires some changes in STA in order to find non deterministic alternatives. In nanoscale CMOS devices, the reduced average number of dopant atoms in the channel of a transistor increases the effect of random dopant fluctuations on the threshold voltage [9].

Increasing levels of process variations have a major impact on power consumption and performance of a design. This impact may result in parametric yield loss [10]. Parametric yield improvement may be achieved by reducing the variability of performance and power consumption of a gate. A high sensitivity of a device to variations in its parameters means that the yield window, limited by frequency and power constraints, is narrower than when a device is more immune to variability. A narrow yield window means that a high quantity of manufactured chips may not satisfy operational specification, leading to a higher cost of fabrication, since many chips may become useless.

It is important to analyze the circuit performance under process variation for yield prediction as well as for circuit optimization. By performing a full-scale transistor-level Monte-Carlo simulation on a circuit, one gets the most accurate way of incorporating the process variation effects into the timing analysis. It generates samples for a given delay distribution and runs a static timing analyzer at each point. The results are put together to form the delay distribution [11].

On the other hand, different logic styles result in transistor networks with different electrical and physical characteristics, and there is usually more than one type of circuit that can be used to represent a certain logic function [12]. The impact of parameters variation of a gate on its metrics is not the same in different logic styles. Also, even for the same logic family, different transistor arrangements result in different electrical behavior under process variation.

The purpose of this work is to evaluate the impact of variation of transistor threshold voltage on CMOS logic gate behavior, according to (i) network topology (transistor arrangement) and (ii) the relative position of the switching transistor in relation to the power supply and output terminals. These data may lead to the development of design guidelines for parametric yield improvement. This paper presents some timing analysis performed on different gates by using electrical simulations.

The paper is organized as follows. Section 2 outlines the methodology applied. Simulation results and analysis are presented in Section 3. In Section 4, the conclusions are then given.

2. Methodology

Transistors threshold voltages (V_{th}) were varied and timing measurements (delay propagation) were taken. The mean delay

* Corresponding author. Tel.: +55 51 3308 6810; fax: +55 51 3308 7308.
E-mail addresses: dnsilva@inf.ufrgs.br, digeorgiasilva@yahoo.com.br (D.N. da Silva).

0026-2714/$ - see front matter © 2009 Elsevier Ltd. All rights reserved.
doi:10.1016/j.microrel.2009.07.023

and standard deviation of the logic gates are then compared, emphasizing the relation of these values to the transistor network arrangements. Timing data were extracted by using Monte-Carlo Spice simulations. CMOS Inverter, 2- to 4-input NAND and NOR, and complex gates (AOI_21 and AOI_32) were used as case studies. Results were obtained from simulations for 3σ deviation of 10% from nominal V_{th}. Correlation between transistors, i.e. that a PMOS may change its parameters when placed in the vicinity of a NMOS was not taken into account. The technology node used in this work was 45 nm and the model file is the Predictive Technology Model (PTM) [13] based on BSIM4. Simulations were carried out by using HSPICE tool.

3. Simulation results and analysis

3.1. CMOS inverter

In a first set of simulations, CMOS inverters were evaluated for different drive strengths while keeping the P/N ratio fixed. Results are presented in Fig. 1. As can be seen, the increasing in the drive strength ($X_1, X_2, \ldots, X_5$) of the inverter results in different behaviors of its metrics and variability. It can be observed in Fig. 1 that the timing behavior directly related to the PMOS transistor (the rise delay deviation) is less impacted by variations in V_{th} than the metric depending directly on the NMOS (the fall delay deviation). The larger the size of the inverter, the smaller the rise delay deviation and the larger the fall delay deviation. It means that falling transitions at the output node of inverters which are placed on the critical paths of the circuits are more critical for parametric yield and timing stability. Such information is quite useful for buffer insertion tasks, for instance.

3.2. NAND and NOR gates

NAND and NOR static CMOS logic gates were also considered for such an investigation since they allows the evaluation of series transistors impact, for pull-up PMOS and pull-down NMOS transistor stacks in NOR and NAND cells, respectively. Usually, timing arcs are taken into account for each input signal transition. Fig. 2a shows rise and fall delay deviations according to the position of switching device in relation to the output node of NAND gates with different number of inputs. Two extreme situations can be identified: (i) when the switching transistor is connected to the cell output terminal ('close' switching) and (ii) when it is connected to the power supply terminal (Vdd or ground) in a stack arrangement

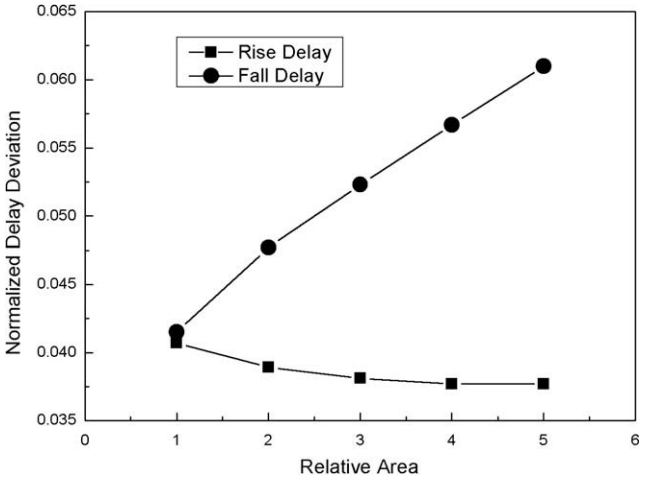

Fig. 1. Normalized rise and fall propagation delay deviations of CMOS inverter by varying drive strength (cell sizing).

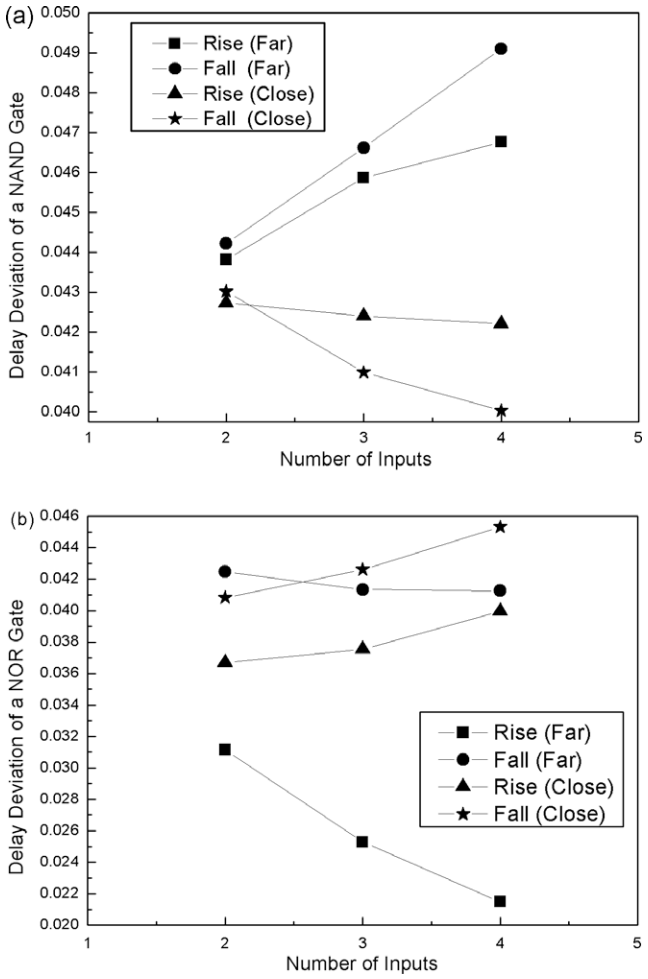

Fig. 2. Normalized rise and fall delay deviations in relation to the number of inputs: (a) NAND and (b) NOR gates.

('far' switching). Transitions close to the logic gate output node result in lower mean rise delay and its deviation than transitions far from such node. In this case, the rise delay deviations obtained are similar for different numbers of inputs. For a signal applied close to the output, fall delay deviation decreases as the number of inputs of the NAND gate increases. The fall and rise delay deviations increase as the number of inputs increases for a transient signal applied far from the output node. Regarding the mean value of delay, there is an increase with the number of inputs, especially when the transient signal is applied far from the output.

In the particular case of NAND gates, lower delay values and delay deviations may be achieved when transient input signals are applied close to the output node. In a transistor stack there are differences in the potential of similar areas of devices, resulting in different gate-to-source (V_{gs}) and drain-to-source (V_{ds}) voltages. Therefore, variations in the threshold voltage may lead to different impact on the drive strength of devices. In NAND gates, the amount of charge that needs to go through a switching transistor far from the output is larger than when it is close to the output, considering other devices in 'on-state'. It helps to explain the dependence of performance variation of the logic gate on the position of the switching transistor.

Fig. 2b shows rise and fall delay deviations for transitions far and close to the output node of a NOR gate. In the case of a switching transistor close to the output node, NOR presents rise delay deviations that increase with the number of inputs. The opposite happens for a switching transistor far from the output node, where