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Breakdown characterization of gate oxides in 35 and 70 Å BCD8 smart power technology

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ABSTRACT

The breakdown of 35 Å and 70 Å thick NMOS and PMOS silicon Gate oxides used in 1.8 V and 3.3 V BCD8 Smart Power technological node was investigated in this work. Both voltage to breakdown, from DC down to the ESD time domain, and time-dependent breakdown analysis have been carried out. We present also the evidence that breakdown is not affected by cumulative stress and it is mainly driven by voltage stress.

1. Introduction

Oxide thickness is one of the most important factor in the definition of the performances of MOSFET based circuits. At the same time, the reduction of the oxide thickness, leading to a reduction of the breakdown voltage, makes more critical the reliability of such structures if exposed to ESD events [1]. Several studies have been proposed in literature regarding the characterization under TLP and vf-TLP regimes of Silicon and high-*k* oxides [2–7]. The main conclusion of such studies is that cumulative effects play an important role in the reaching of the breakdown point for tested dielectrics. We have tested 35 Å and 70 Å oxides of NMOS and PMOS Smart Power BCD8 technology (respectively, for 1.8 and 3.3 V), with DC, pulsed regime (TLP), and TDDB setups, obtaining different results with respect to the previous works, but comparable with to each other considering the three different measurement setups. Then, this work wants to be a starting point for the investigation of the Safe Operating Area, essential for the design of proper EOS/ESD protection structures from ESD time domain (from sub-nanoseconds range typical of Charged Device Model, up to some hundreds of nanoseconds like during Human Body Model stress), up to DC regime.

2. Device description and measurement setups

The work was based on NMOS (poly N+/Pwell) and PMOS (poly P+/Nwell) transistors with oxide thickness of 35 Å and 70 Å. Devices dimensions were width = 100 μm (W) and length = 100 μm (L), relatively big in order to minimize the perimeter impact on the overall dielectric breakdown. Tested devices were designed with 150 μm GSG pads configuration, in order to make possible the testing with high frequencies probes, necessary for the breakdown characterization on the ESD time domain (some nanoseconds). All tests were performed stressing the Gate pad, with the Drain, Source, and Body contacts shorted to ground. Considering NMOS devices, measurements were performed in both inversion ($V_G > 0$ V) and in accumulation ($V_G < 0$ V), and vice versa concerning PMOS structures. Three different measurement setups have been developed for this work: (i) DC characterization, (ii) pulsed voltage to breakdown (VTB) analysis, and (iii) time-dependant dielectric breakdown (TDDB) investigation. In both the pulsed regime setups, adopted failure criterion was the oxide leakage current, measured at 1.8 V and 3.3 V, respectively, for 35 Å and 70 Å dielectric thickness.

Initial DC characterization: (i) were performed with an Hp 4145 semiconductor parameter analyzer and a Keithley 2612 source meter, obtaining similar results. Stair-like voltage stress was applied to the Device Under Test (DUT) up to the reaching of the breakdown point. The duration of each step was about 48 ms, measured with the time-stamping function of the Keithley 2612 (integration time = NPLC = 1, in the middle between Agilent "medium" and "long" integration time). Anyway, we have verified that the integration time does not influence the measurement, obtaining identical *I–V* curves.

Pulsed regime measurements (ii) were performed by means of a 100 ns Transmission Line Pulser (TLP-TDR, [9]), that is a widely used characterization tool for both ESD-like, and pulsed regime characterization. The setup, based on the Time Domain Reflectometer technique, produces square-shaped pulses with sub-nanosecond rise time with a 50 Ω line impedance. Voltage and current (Tektronix CT-1, 5 mV/mm ac-current probe) waveforms were acquired for each step. A similar setup, but based on a Hp 8114A solid state pulser was also used, in order to characterize the dielectric

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breakdown from 20 ns up to ms regime. The voltage drop on a 1 KΩ resistor was used to measure the current with pulses longer than 1 μs, because of the limitation of the CT-1 ac-current probe. Pulsed measurements longer than 200 μs were also carried out with the Keithley 2612, in order to validate the setup, obtaining good results.

The time dependence to breakdown (TDDB) (iii) of studied devices was investigated developing a setup based on the solid state pulser Hp 8114A, and a Tektronix TDS6804B DSO (analog bandwidth = 8 GHz, 20 GSample/s). A schematic of the adopted setup is shown in Fig. 1.

Preliminary measurements were carried out placing both voltage and current probes very close to the rf tip (below 1 cm) in order to reduce the impact of signal reflections on the extraction of the breakdown time. An example of the voltage and current waveforms acquired is shown in Fig. 2.

The breakdown condition is clearly detectable with the abrupt decrease of the voltage waveform (after about 14 μs), or increase of the current pulse. Because of the current signal did not give more information than the voltage signal on the occurrence of the breakdown point, it was removed from the final TDDB setup, in order to further reduce parasitic effects.

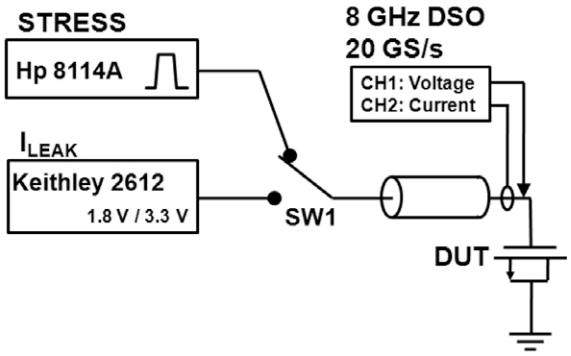

Fig. 1. Schematic of the setup used for TDDB investigations. The ac-current probe was then removed, to further reduce parasitic effects.

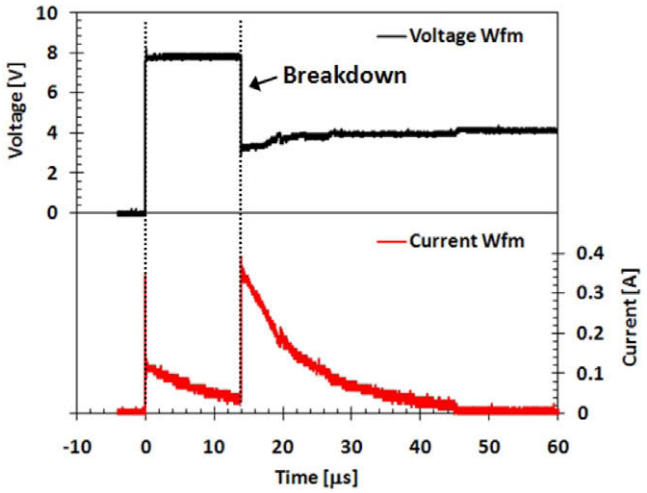

Fig. 2. Voltage (top, black) and current (bottom, red) waveforms measured during TDDB investigations. The breakdown occurrence is also highlighted. DSO time resolution was 400 ps/pt. The decay of the current waveform was due to the high-pass behavior of the ac-current probe. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

3. Experimental results

3.1. DC-regime characterization

We have used the DC-setup (i) in order to make a preliminary characterization of oxides main electrical parameters. Figs. 3 and 4, respectively, show the DC-regime characterization of NMOS and PMOS oxides (35 Å and 70 Å thick) under POSITIVE and NEGATIVE voltage stress.

POSITIVE DC failure voltage values were: NMOS 35 Å = 5.8 V, PMOS 35 Å = 5.8 V, NMOS 70 Å = 11.5 V, PMOS 70 Å = 12.5 V.

NEGATIVE DC failure voltage values were: NMOS 35 Å = −6.1 V, PMOS 35 Å = −6.3 V, NMOS 70 Å = −11.5 V, PMOS 70 Å = −12.5 V.

From Figs. 3 and 4 it is possible to note that PMOS devices have shown a slight higher robustness than NMOS ones. This behavior has been reported also in [6], as due to the greater parasitic series resistance of PMOS devices. However, because of the very low current values (at 1 nA the voltage difference is about 1 V), this should not be assumed as the main cause of the difference between NMOS and PMOS devices robustness. Actually, the difference in flat-band voltages of NMOS and PMOS devices could be the responsible of the observed shift robustness.

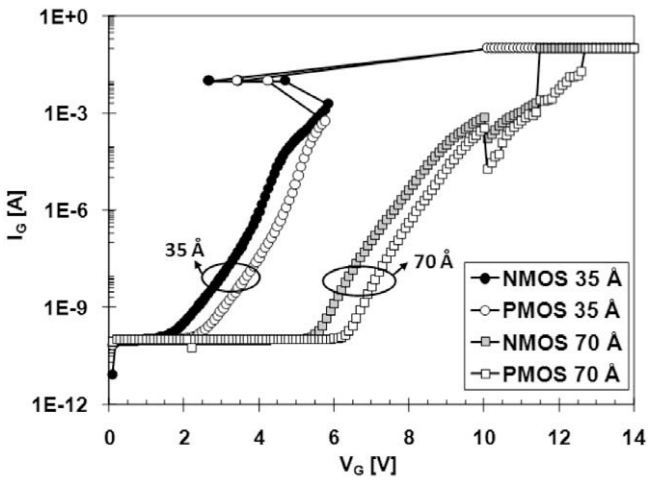

Fig. 3. *I–V* curves of 35 Å and 70 Å thick N- and PMOS oxides measured in DC regime under POSITIVE voltage stress (current compliance level = 100 mA).

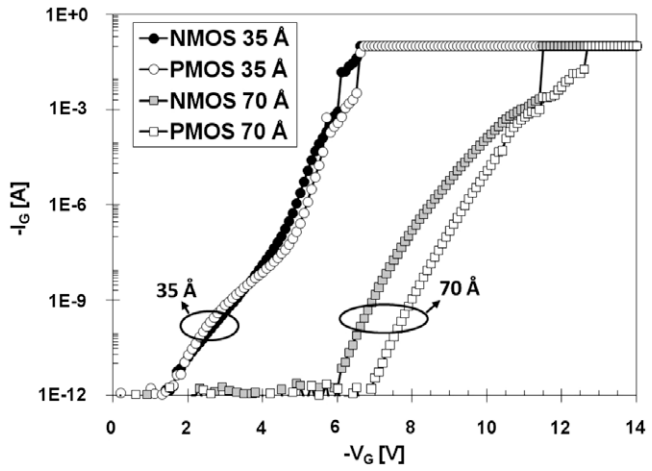

Fig. 4. *I–V* curves of 35 Å and 70 Å thick N- and PMOS oxides measured in DC regime under NEGATIVE voltage stress (current compliance level = 100 mA).