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Jitter analysis of PLL-generated clock propagation using Jitter Mitigation techniques with laser voltage probing

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ABSTRACT

A new Jitter Mitigation feature in the latest generation laser voltage probing (LVP) tool effectively removes PLL jitter from LVP waveforms [Ng Yin S, Lo W, Wilsher K. Next generation laser voltage probing. In: Proceeding, international symposium on testing and failure analysis; 2008. p. 249]. It facilitates the probing of phase-locked loop (PLL) driven circuitry inside of integrated circuits (ICs). In particular, it allows the detection of small amounts of excess jitter that would normally be masked by the much larger jitter of the PLL. To demonstrate the practical application of this Jitter Mitigation feature, we report on the jitter analysis of a PLL-generated clock signal as it propagates, through buffers and logic circuitry, to an external I/O pad of an IC. The IC was a 0.9 V, 65 nm technology graphics processing unit (GPU). The analysis was to determine where excess jitter was introduced into the clock path when the GPU was electrically stressed. Details of the jitter analysis, including Jitter Mitigation methodology, probing setup, and results of the timing measurements, will be presented in this paper.

1. Introduction

Excess jitter was found on one of the clock outputs of a GPU when it was electrically stressed. Electrical characterization of the GPU revealed that the other clock outputs generated by the same PLL did not exhibit excess jitter. This indicated that the excess jitter was not generated in the PLL itself, but was injected somewhere along the clock signal path. Period jitter measurements made electrically at the external I/O pin showed that jitter increased from 37 ps (full width at half maximum, FWHM) in idle mode, to 54 ps when the chip was fully stressed. Assuming random jitter sources, the excess jitter is calculated to be: $\sqrt{(54\text{ ps})^2 - (37\text{ ps})^2} = 39\text{ ps}$ (FWHM).

An LVP analysis was undertaken to identify the location along the internal clock path where this extra 39 ps of jitter was introduced. The latest generation LVP tool was selected because of its new Jitter Mitigation feature, its high intrinsic bandwidth (up to 20 GHz) and its low-voltage probing capabilities ($V_{dd} < 0.5$ V).

In traditional LVP, the signal of interest is acquired in reference to a separate electrical trigger signal that is provided to the probing tool [2]. This trigger is usually generated by an automated test equipment (ATE) tester, or is derived from the crystal oscillator of a system applications board (hereafter, both will be referred to as the device under test stimulus). The stimulus also provides the reference clock signal to the device under test (DUT). The trigger signal is therefore synchronous with, and coherent to, the DUT's reference clock.

On-chip PLLs are typically used to derive higher frequency core-clock signals from the provided reference clock. Since PLLs invariably introduces jitter between its reference and output clock signals, waveforms acquired using a traditional LVP tool on circuits driven by a PLL will have the PLL's jitter embedded in the acquisition. Because PLL jitter is usually the dominant form of jitter in a chip, it can mask the jitter from other sources.

Jitter Mitigation provides a solution to this problem by enabling the LVP system to be triggered by an edge of another clock reference. This new clock effectively becomes the timing reference and all jitter measurements are made relative to that clock. For example, if a direct output from the PLL is available, the PLL clock can become the timing reference for LVP measurements.

In this paper we took a slightly different approach. As a direct output of the PLL was not available, the output of the clock tree that was exhibiting the excess jitter was used as the timing reference, requiring us to work backwards towards the jitter source. Details are presented in the following sections.

2. Period jitter

Period jitter (Fig. 1) is defined as the maximum change in a clock's output transition from its average, and is typically quoted

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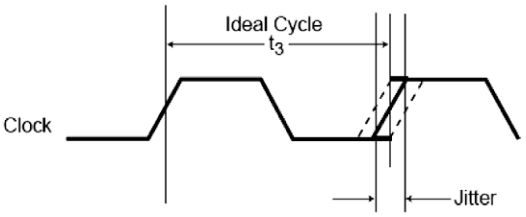

Fig. 1. Definition of period jitter: the deviation of the period from the average period.

as a peak-to-peak value for deterministic jitter to indicate the maximum change in the clock period. Root mean square (RMS) values are typically used if the jitter source is random. Random jitter follows a normal distribution and is not bounded by a simple peak-to-peak value.

Period jitter is measured electrically using an oscilloscope by triggering on one clock edge and setting the time-base parameters to display the next corresponding edge. Traces are accumulated using a long persistence value of the oscilloscope and a histogram is generated of the crossing point of the edge. Jitter parameters, including peak-to-peak and RMS values, are given by the histogram statistics generated by the oscilloscope (see Fig. 2).

3. Measuring jitter with LVP

There are several key differences between measuring period jitter on an oscilloscope, and measuring jitter using Jitter Mitigation on an LVP tool.

First, the oscilloscope is capable of being triggered by the signal being measured itself while the LVP tool requires a separate electrical signal to generate the trigger. This difference means that LVP waveforms are sensitive to jitter introduced on the electrical trigger signal path as well as to jitter introduced on the signal path of interest. To separate the two contributions, the jitter on the trigger signal path itself can be first characterized by LVP probing. This limitation did not impact our analysis because the signal path of interest was driving an I/O pad, which we were able to trigger on.

Second, the particular clock edge that the oscilloscope triggers on is random, so that all possible clock periods can be (eventually) captured. The LVP tool, on the other hand, requires a fixed trigger period (i.e., loop length), and, therefore, may not sample all possible clock periods. Thus, the LVP jitter measurement may not give the true extent of jitter in the signal. This limitation did not impact our analysis because our approach did not require measuring the true extent of jitter, only the relative jitter difference between two modes of chip operation.

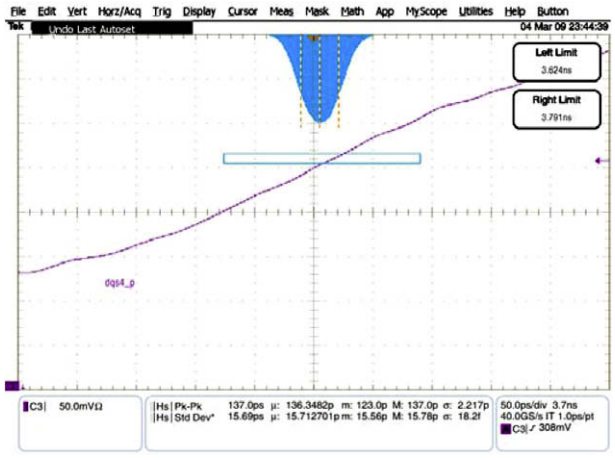

Fig. 2. Histogram measurements of a rising edge of the GPU clock signal to characterize period jitter on the device's external output. RMS (i.e., standard deviation) value of jitter is 15.7 ps. Converting to FWHM (by multiplying by 2.35 for a normal distribution) gives 37 ps jitter.

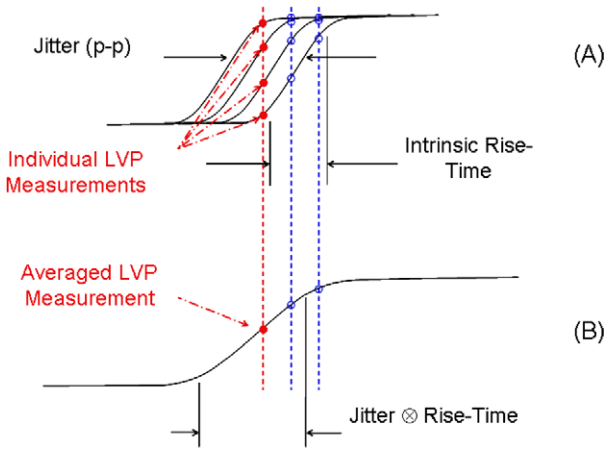

Fig. 3. Diagram illustrating how jitter convolves with signal rise-time in LVP waveforms due to averaging: (A) shows a jittery edge that is sampled by the LVP tool over multiple repetitions of the signal and (B) shows the resultant LVP waveform in which each point is generated by averaging the individual measurements. LVP measured rise-time is degraded by the jitter.

Finally, a single LVP measurement has signal-to-noise ratio (SNR) $\ll 1$ (which is why the LVP tool can not be directly triggered by the signal being measured) so single-shot LVP waveform captures are not possible. To achieve a useful SNR in the final LVP waveform, many individual measurements must be averaged together. Unfortunately, averaging prevents jitter from being directly detected in the LVP waveforms: jitter is convolved with the measured rise/fall time of the node being probed and can only be detected through its effect on waveform rise/fall times (see Figs. 3 and 6).

Several factors influence the measured rise/fall time of the LVP waveforms: (1) The intrinsic rise or fall time of the node, t_{Switch}; (2) the step response time of the LVP tool, t_{lvp} (=0.35/BW, where BW is the tool bandwidth); and (3) jitter, including PLL jitter and any excess jitter caused by signal cross-talk, etc.: J_{PLL} and J_{Excess}.

All of these components convolve together to give the rise/fall time of the acquired LVP waveform. Assuming Gaussian response for all components (random jitter, Gaussian frequency response of the LVP system, and Gaussian-integral edge profile[1]), the rise/fall time, $t_{R/F}$, of the acquired waveform is given by adding all of the contributions in quadrature:

$$t_{R/T} = \sqrt{(t_{LVP})^2 + (t_{Switch})^2 + (J_{PLL})^2 + (J_{Excess})^2} \quad (1)$$

where J_{PLL} and J_{Excess} are FWHM measurements of the corresponding jitter distribution, and all rise/fall time measurements are 20–80% values.[2] Since all of these factors convolve together to affect the measured rise/fall time, detecting a small amount of excess jitter requires reducing the contributions from all other factors as much as

[1] That is, the edge is assumed to be modeled using an error function, erf(x). In practice, edges are fitted to a hyperbolic tangent function, tanh(x), using the LVP tool. Assumption of an erf(x) fit is justified here since the differences are minor in the context of this discussion.

[2] More properly, the rise-times should be measured from 24% to 76% points to match the FWHM measurements of the other factors. However, 20–80% rise/fall time measurements are more common, and the error in using 20–80% values is <10%, which is not significant in the context of the discussion.