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Thermal imaging of smart power DMOS transistors in the thermally unstable regime using a compact transient interferometric mapping system

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ABSTRACT

Smart power DMOSes are analyzed under thermally unstable conditions up to the destruction level using a new compact version of the transient interferometric mapping (TIM) method. High accuracy phase measurements are achieved employing superluminescent diodes and focal plane array cameras. Two-dimensional thermal mapping at two time instants during a single stress pulse is performed in the range of 100 μs to few milliseconds. The size of the region where the parasitic bipolar transistor becomes thermally activated at the onset of thermal runaway is determined. The results are correlated to conventional failure analysis.

1. Introduction

Due to continuing shrinkage of feature size and enhancement of integration density double-diffused power MOSFET (DMOS) devices have to handle more and more power dissipation density [1–3]. It is well known that for the gate to source bias V_{gs} below the so-called temperature compensation point (TCP) the drain current increases with temperature, which may lead to thermal instability resulting in catastrophic failure due to a local hot spot [4]. The temperature rise due to positive thermo-electrical feedback can lead to the activation of a parasitic bipolar transistor inherent to the DMOS structure or directly to the body-drain pn junction thermal runaway due to thermal carrier generation [1,2,4–7]. For the verification and calibration of electro-thermal simulation tools [2,6–9] it is therefore important to have experimental information about the thermal distribution as close as possible to the time of destruction. Infrared (IR) thermography has previously been used to characterize surface temperature under thermally unstable conditions in DMOS [1,6]. The transient interferometric mapping (TIM) method [10,11] has shown its single shot imaging capability for the investigation of thermal distribution in electrostatic discharge (ESD) protection devices including destructive pulses and in DMOSes under ESD conditions [12,13] or for thermal mapping of power DMOS drivers under short circuit conditions in the 10 μs to milliseconds time scale [14]. IR thermography and TIM are complementary techniques. While the former measures directly the surface temperature which may however differ at short time scale from the silicon temperature due to top metal or passivation layers, the latter probes the heat energy in the bulk silicon.

Here we investigate small and large DMOS devices under high current short circuit conditions. Thermal imaging is performed also under thermally unstable conditions, up to the device destruction. For this purpose we have developed a compact imaging system based on the TIM method variant used previously for leakage current analysis [15]. The thermal images during destructive pulses are correlated with failure analysis.

2. Experiments

2.1. Devices

Small and big area vertical DMOS devices of a smart power technology are examined [2]. The big device is composed of five large area finger blocks, where only a middle block is actively controlled by gate, while the others have the gate grounded.

For the experiments the samples are backside polished and glued to a printed circuit board which allows access to both the frontside for bonding and the backside for optical investigations.

2.2. Electrical methods

The electrical device connections are shown in Fig. 1. The drain voltage is provided by a DC source and a 1 mF capacity to keep a constant voltage. The gate is pulsed with a HP 214B pulser. TCP of V_{gs} = 2.4 V was determined from DC measurements using a temperature controlled chuck. Voltage is measured with high impedance probes, for measurement of the drain current an Agilent

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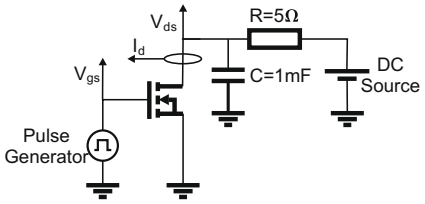

Fig. 1. Electrical device connection.

N2774A current probe with a bandwidth from DC to 50 MHz is used.

2.3. Optical methods

2D thermal imaging is performed using a 2D TIM system, which has originally been developed for measurements of small repetitive signals [15]. TIM monitors transient phase changes in an IR laser beam probing the device from the backside [10]. The phase of a beam reflected at topside oxide and metallization layers is influenced by free carriers (plasma-optical effect) and temperature (thermo-optical effect). In the present case the positive contribution of the thermo-optical effect is dominant.

2D TIM is based on holographic interferometry and is using an equal-path Michelson interferometer. The enhancement of the existing setup includes the implementation of a second interferometer allowing to measure two images at two InGaAs focal plane array (FPA) IR cameras simultaneously. Two orthogonally polarized beams from two superluminescent diodes (SLDs) are chopped by acousto-optical modulators (AOMs) to provide measurements at two time instants during a single pulse. The orthogonal polarization of the beams is achieved by polarizing beam splitters (see Fig. 2).

Compared to the previous 2D TIM setup for imaging at two time instants (i.e. the setup for ESD analysis [11]) the advantage of the new system is its compactness (avoiding large water-cooled high energy laser sources), and a high low-frequency mechanical stability which together with the high pulse to pulse stability improves the phase accuracy. The time resolution under single shot operation is 20 μs which is limited by the speed of the AOM, the single-pulse detection limit of the camera and the SLD power. This is however sufficient for thermal imaging in the time scale of 100 μs to 10 ms including detection under destructive pulses in this work. The field of view can be chosen between 250 μm × 300 μm and 2.5 mm × 3 mm. Under the smallest field of view, the achievable spatial resolution of the setup is 1.9 μm, limited by diffraction.

In addition to the 2D SLD setup a scanning heterodyne interferometer [16] has been used for transient measurements for phase calibration purpose.

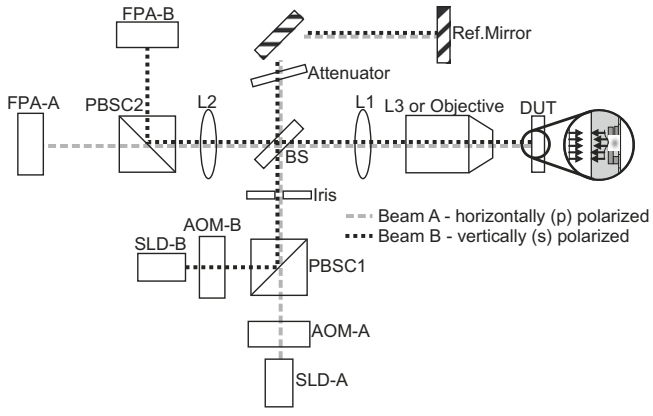

Fig. 2. Schematic of the optical setup. The abbreviations are: SLD: superluminescent diode, AOM: acousto-optical modulator, PBSC: polarizing beam splitter cube, BS: beam splitter, L: lens, DUT: device under test, FPA: focal plane array camera.

3. Results and discussion

3.1. Small DMOS device

A typical backside IR reflectivity image of a small device is given in Fig. 3a. Thermal images of the small DMOS device were recorded at and above TCP for different drain voltages and pulse durations. Fig. 3b–g shows extracted phase images and Fig. 4 phase cross sections at the vertical line from Fig. 3a. Even at high power dissipation (2.5 W), i.e. at $V_{gs} \gg V_{gs,TCP}$, it was not possible to degrade the device up to pulse durations of 10 ms. This is due to a good lateral heat removal from the device.

3.2. Big DMOS device

The big DMOS device was analyzed below TCP (i.e. $V_{gs} < V_{gs,TCP}$). Thermal inspection of the big DMOS with a large field of view (see Fig. 5) revealed that a magnification of the middle part of the central finger block is necessary in order to resolve the size of the region where the thermal runaway is initiated. Therefore further detailed investigations have been performed under larger magnification (see Figs. 6–8).

Due to an absence of phase reference in the zoomed image (i.e. the whole zoomed area is heated) there arises a $N * 2\pi$ uncertainty in the absolute phase value in the image ($N = 1, 2, \ldots$). Therefore the extracted phase profile maxima (see Fig. 8) were calibrated using measurements with the heterodyne scanning interferometer recorded in the central part of the device. Due to different thermal conditions caused by sample mounting and a high sensitivity of the time to failure on the exact settings of gate and drain voltage, destruction occurred at different time instants in the heterodyne and in the SLD setup. Therefore the calibration was done by extrapolation of the phase shift during a non-destructive pulse (see Fig. 9).

The pulse duration in the 2D TIM measurements was increased until the device was destroyed at about 1 ms. Before destruction the drain current increases due to positive thermal feedback until finally thermal runaway occurs. A typical current transient aligned to the gate voltage pulse is given in Fig. 10.

The extracted phase shift for different pulse lengths up to the destruction level is given in Fig. 7 (2D TIM images) and Fig. 8 (cross sections). In the phase image recorded during the destructive pulse a pronounced increase of the phase shift in the center of the device is visible (see the curves at $t = 1060$ μs in Fig. 8), corresponding to increased power dissipation. The size of this thermal-runaway area is approximately 40 μm × 50 μm which is important information for thermal model calibration [2]. At this region the thermal carrier generation takes place activating the parasitic bipolar transistor.

The interferogram corresponding to the image at the destruction level exhibits a blurred region which can be seen in the center of the image (see Fig. 6). This blurring probably occurs due to a rapid change in the phase shift and partial fringe intensity averaging during the 20 μs long imaging light pulse or due to absorption by free carriers. So it is possible to extract the size of the thermal-runaway area even from the interferogram.

As soon as the thermal runaway occurs the device is not controllable by the gate potential anymore, leading to a catastrophic destruction. Fig. 11 shows a backside IR image of the DMOS with recognizable damage in the central region. A damage in the power