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An AC–DC converter for human body-based vibration energy harvesting

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ABSTRACT

This paper presents an optimized AC–DC converter designed in 65 nm low power process technology. Two topologies of the AC–DC converter are designed, namely, Bias-Flip rectifier and Voltage Doubler. The design is part of a piezo electric energy harvesting system targeting wearable electronics. Voltage doubler and full-bridge rectifier are fabricated to support a start-up mechanism while the bias-flip rectifier supports higher efficiency for the normal operation mode. Using a piezo electric energy harvester mounted on a shaker and operated at 4.5 Hz, the maximum extracted power from the voltage doubler is measured as 79.8 nW at 0.21 g. In addition, the maximum extracted power from the full-bridge rectifier is measured as 22.2 nW. As such, voltage doubler is more efficient than full-bridge rectifier by 71%. The experiment uses MIDE V22BL piezo electric harvester with 25 Hz resonance frequency. However, the harvester was used at 4.5 Hz (human frequency) which degrade the energy extracted from the harvester. If another harvester was designed to tune to lower frequency, higher energy level can be extracted. Another contribution in this paper is to compare the on-chip voltage doubler to board level with discrete components. Our experimental results show 11% improvement in efficiency for the on-chip design compared to off-chip for the same input power. The combined bias-flip rectifier and voltage doubler support energy autonomous systems where no start-up power is needed.

1. Introduction

Emerging technology in semiconductor devices and circuits has enabled ultra-low power systems in medical, smart structures, and hard to reach places which fueled the energy scavenging research [1–3]. Energy harvesting could play an important role in biomedical devices where it extends the lifetime of the system, and eliminates the need for periodic maintenance such as exchanging or recharging the battery. Energy can be harvested from ambient sources such as solar light [4], radio [5], heat [6] and vibrations [7]. In particular, thermal and vibration energy generated from human body are harvested using Thermoelectric Generator (TEG) and Piezo Electric (PE) energy harvester, respectively. Human body-based thermal and vibration energy harvesting has been of recent interest in powering biomedical electronics for their almost universal availability [8]. Experimental results of vibration energy harvested from human body movement using PE harvester are reported in [9]. The reported range of the PE harvester open circuit voltage is from 0.84 V to 7.68 V at different human speeds. As such, the expected output voltage from human vibrations can reach up to 8 V. This should be taken into consideration when designing the interface circuit in order not to exceed the breakdown voltage of the transistor.

This research focuses on harvesting vibration energy generated from human body movement using the piezo electric energy harvester. A special interface circuit is required to extract, convert, and condition the harvested voltage to be utilized by the load. This paper presents two AC–DC converters, the Voltage Doubler (VD) and the Bias-Flip (BF) rectifier. Compared to common topologies of AC–DC converters, VD has moderate efficiency, small area (two diodes only), and no additional circuits to operate [10]. On the other hand, BF rectifier has higher efficiency compared to VD, larger area (four diodes+switch+inductor (off-chip)), and requires additional circuits [10]. BF rectifier is actually obtained from Full-Bridge (FB) rectifier in addition to a switch and an inductor [11]. Compared to VD and BF rectifier, FB rectifier has lower efficiency, moderate area (four diodes), and does not require any additional circuits [12]. Unlike VD, power conversion circuit in FB rectifier does not share common ground with PE harvester. VD and FB rectifier are good candidates for start-up mode operation of DC–DC converters as they are passive rectifiers.

The start-up cycle in Fig. 1 starts by harvesting vibration energy

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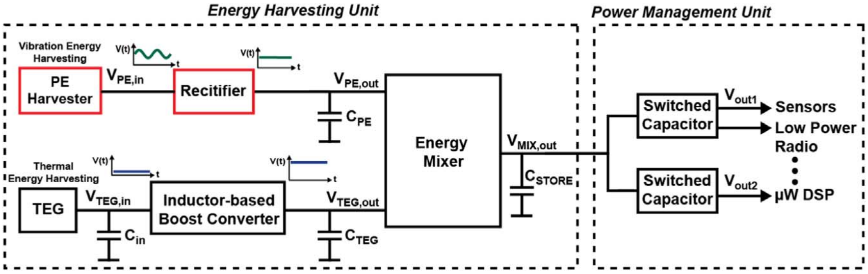

Fig. 1. TEG and PE energy harvesting systems block diagram during start-up.

using PE harvester, as it has higher voltage compared to TEG, then rectifying the harvested voltage using the AC–DC rectifier (VD or FB), and storing the energy in a storage element. Note that the outputs of the rectifier and the boost converter are of the same type (DC voltage), which are fed to the energy mixer to efficiently select the transferred energy into the main storage. When sufficient energy is available, both of DC–DC converter and AC–DC converter will work simultaneously. In situations where harvested energy is insufficient, the system puts AC–DC converter in action instead of the DC–DC converter. This operation will remain until the harvested energy is higher than the threshold value.

Ref. [4] proposed a platform architecture that combines energy from three sources of energy: solar, thermal, and vibration. This platform is fabricated using 0.35 μm CMOS technology process. The vibration energy-harvesting source in this work is the PE harvester. The AC–DC converter that is responsible of rectifying PE's output is a VD rectifier. PE harvester along with the rectifier can be modeled as a DC voltage source in series with a resistor that represents the internal impedance of the PE harvester. Maximum output power from the PE harvester can be extracted if the internal impedance of the harvester is equal to the internal impedance of the PE harvester interface circuit. Since the resistor in PE harvester model has constant value over the harvester's operating range, the harvester interface circuit requires a one-time impedance tuning. In order to suppress ripples in the rectified voltage, 1 μF capacitor is connected at the output of the rectifier. Measured output ripple for the PE harvester interface circuit is less than 20 mV. In addition, measured output voltage from the PE harvester is 2.5 V.

Besides, Ref. [7] proposed a self-powered rectifier for PE harvesting applications. The proposed rectifier consists of two switches and two active diodes that are based on op-amps. The rectifier is fabricated using 0.18 μm CMOS technology. Power efficiency is measured as 91.2 % and the extracted power is greater than conventional rectifiers by 3.5 times.

The remainder of the paper is organized as follows. Section 2 provides overview of the energy-autonomous wearable biomedical system. Section 3 explains the process of optimizing, designing, and analyzing VD and BF rectifier. Section 4 discusses experimental setup and obtained measurements. Finally, Section 5 concludes the paper.

2. Self-powered system overview

This research is part of an energy-autonomous wearable biomedical system that utilizes sensors to measure vital signs from the human body. The integrated biomedical processor system is fully described in [13] where a block level diagram of the proposed non-invasive health monitoring system for diabetics is illustrated. The main blocks in this system are energy harvesting and power management, biomedical sensors, biomedical processor, and wireless transmitter. Fig. 1 illustrates the block diagram for the energy harvesting and power management units. These units have two energy harvesting sources (TEG and PE harvester), interface circuits, energy mixer, and a storage element. The rectifier and the inductor-based boost converter are interface circuits for PE harvester and TEG, respectively. Energy mixer efficiently combines, selects, and transfers the harvested energy into the main storage. Finally, power management unit drives each load with suitable voltage level while maintaining low power and minimum leakage operation.

3. AC–DC converter design and analysis

In this section, detailed design analysis and size selection of rectifying diodes will be discussed. As mentioned in Section 1, VD and FB rectifier can be used during start-up mode operation. Fig. 2 illustrates PE harvester model and VD schematic. The illustrated PE harvester model is based on cantilever design at resonance [11]. Note that MOS transistors are used as diode-connected devices for their low threshold voltages [14].

Both interface circuits are fully-designed in 65 nm CMOS process using thick oxide pMOS transistors. It can be depicted in Fig. 2 that anode of the diode is the source terminal in pMOS transistor, and cathode is obtained by shorting gate, drain and bulk terminals. Because of CMOS technology, gate oxide of the used transistor can tolerate up to 3.3 V only. However, maximum expected output voltage from human vibrations can reach up to 8 V [9]. Since gate terminal is connected to output node, the circuit can be protected by limiting the output voltage to 3 V maximum. This way, the issue of having high voltage at the gate terminal can be avoided.

Table 1 lists the values of the parameters shown in Fig. 2. Ref. [9] reported maximum measured frequency of human vibrations as 1.47 Hz at 7 mi/h. As such, frequency of the sinusoidal current source (f_s) is set to 2 Hz, and the current (I_P) is set to 2.8 μA. This particular value of I_P is chosen after adjusting open circuit output voltage of PE harvester model to 7.68 V. Moreover, [9] reported measured value of parasitic capacitance (C_P) as 4.6 nF. In addition, the parasitic resistance (R_P) is considered to be trivially large at low frequency vibrations [15]. Finally, C_{RECT} is the output capacitor which has a value of 1 μF.

To choose the width of diode-connected pMOS (W_{pMOS}), its effect on the voltage drop across the MOS (V_{DT}), and leakage current ($I_{leakage}$) are investigated. Diode-connected pMOS should be sized to achieve the lowest possible V_{DT} and $I_{leakage}$. Fig. 3(a) and (b) shows diode-connected pMOS in forward bias region and reverse bias region, respectively. Voltage drop across the MOS (V_{DT}) is measured in forward bias region, and $I_{leakage}$ is measured in reverse bias region.

Effect of W_{pMOS} on V_{DT} and $I_{leakage}$ is illustrated in Fig. 4. As depicted in the figure, increasing the width of the transistor decreases voltage drop across the MOS (V_{DT}). As channel width increases, channel resistance decreases and thereby, voltage drop decreases. In addition, increasing W_{pMOS} from 0.4 μm to