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Development of a simulator for analyzing some performance parameters of nanoscale strained silicon MOSFET-based CMOS inverters

Subindu Kumar*, Amrita Kumari, Mukul Kumar Das

Department of Electronics Engineering, Indian School of Mines, Dhanbad, Jharkhand 826004, India

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ABSTRACT

Owing to the persisting technological importance of Strained-Si (S–Si) metal-oxide-semiconductor field-effect transistors (MOSFETs) and the hurdles offered by source (S) and drain (D) series resistances in the nanometer regime, a simulator has been developed for evaluating the voltage transfer characteristics (VTC) and analyzing some performance parameters of such devices-based CMOS inverters. The algorithms used for framing the simulator are based on analytical equations which can accurately estimate the noise margin (NM), dynamic current, and so on. The effects of strain on the circuit performance have also been investigated, with emphasis on the variations of drain current dependent transconductance ratio. A scope of using high-k dielectric materials along with strain is also explored. The algorithms proposed in this work are not only restricted to strained-Si MOSFETs but can also be applied to any novel device structure and complex digital logics, presented as case studies.

1. Introduction

Strain was introduced in the 90 nm technology node which led to the improvement of metal-oxide-semiconductor field-effect transistor (MOSFET) performance without scaling [1–3]. A comprehensive review of strain engineering can be found in [4]. Use of commercial circuit simulators [5,6] and Technology Computer Aided Design (TCAD) tools [7,8] for analyzing the performance parameters of circuits comprising of strained/unstrained devices is now one of the common practices. Beyond doubt, such simulators and TCAD tools plays an important role in coming up with optimized device designs having different geometries and materials. Various device physics models such as Drift-Diffusion, Boltzmann (Monte Carlo), Hydrodynamics, Quantum Corrected Boltzmann, Non-equilibrium Greens Function, and so on have been employed in these tools to have an approximate prediction of the behaviour of semiconductor devices [9] by solving large number of partial differential equation with appropriate boundary conditions. A number of discretization techniques such as Finite Difference Method (FDM), Finite Element Method (FEM), Finite Volume Method (FVM), and so on [10] have also been used as backbones of TCAD tools. These underlining mechanisms of computation are not of much concern to the user. However, as device dimensions enter into the nanometer regime, TCAD tools are pushed to the limits of their applicability [9] and methods have been suggested [11] for refining of these tools. Furthermore, there is always a lack of consensus in the research community as to which analytical model is most physically sound and makes most accurate predictions [12]. At this juncture, presenting a computational technique for nanoscale strained-Si (NS-Si)-based circuits, based on successive iteration of analytical equations, but still giving accurate results, may be useful to the scientific community. Such approach has not been widely discussed or analyzed. Voltage transfer characteristics (VTC) of S-Si MOSFET-based CMOS inverters have been investigated for several decades [13–17]. To mention few, primary works include the experimental studies of Hwang et al. [13] on the VTC of 70 nm S–Si CMOS on SiGe virtual substrate. Alatise et al. [14] used the thickness of SiGe relaxed layer to tune the VTC of CMOS circuits. Studies on the impact of strain on the VTC of NS-Si MOSFET-based circuits with the help of TCAD tools was explored by Ramakrishnan et al. [15,16]. Recently, we have proposed a preliminary technique for analyzing the VTC curves of nanoscale MOSFET-based circuits without incorporating the adverse effects of source (S)/drain (D) series resistance [17].

Keeping in mind the technological hurdles offered by the S/D series resistance [18–20] in the nanometer regime which forces the drain current to take the form of a transcendental equation, a simulator has been developed for analyzing the VTC and evaluating the noise margin (NM), inverter logic threshold voltage (V_{inv}) and dynamic current (I_{CC}) of NS-Si MOSFET-based CMOS inverters.

* Corresponding author.
E-mail address: subindukumar@hotmail.com (S. Kumar).

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The framework of our algorithm is based on S–Si/relaxed-$Si_{1-x}Ge_x$ MOSFETs, which are still of technological importance [21–24]. All aspects of the proposed algorithms have been discussed in-depth with proper validation. To test the universality of our technique, we have applied the proposed method on a complex digital logic and strained-Si/strained-$Si_{1-y}Ge_y$/relaxed-$Si_{1-x}Ge_x$ MOSFET-based circuits. The computations are also extended to devices having high-k dielectric materials. The proposed technique is transparent and uses one kernel which makes it computationally less expensive than Monte Carlo simulation [25], finite element analysis [26], and so on, and can be applied to any novel device structure, signifying it's flexibility.

2. The strained si/$Si_{1-x}Ge_x$ MOSFET

Fig. 1a is a generic representation of the cross-section of n-channel strained-Si/relaxed $Si_{1-x}Ge_x$ MOSFET. Modifications in the practical and fabricated device structure to encounter various small dimensional effects are not shown in this figure. Such effects will be considered at a later stage during the formulation of the model. Fig. 1b shows the schematic representation of a S–Si MOSFET under various bias conditions along with S/D series resistance (R_S and R_D) as it is equally important for strained devices [3,20,27]. It may be felt that extending S/D regions deep into the substrate can lower the S/D series resistance. But we would like to mention at this juncture that even for conventional/strained MOSFETs, in order to keep pace with the scaling trends, the S/D penetration depth into the substrate has also been scaled proportionally along with the channel length, with a motivation to reduce short channel effects. Thus it becomes necessary to consider the effects of S/D series resistance in strained devices. The schematic diagram of a generalized CMOS inverter utilizing strained devices, incorporating S/D series resistance is depicted in Fig. 1c. The subscript '*int*' associated with various terminal voltages represents the intrinsic parameter of the device. In presence of $R_{S(D)}$, the intrinsic voltages can be represented as

$$V_{DS,\,\mathrm{int}} = V_{DS,n} - I_{D,n}R_{SD,n} \tag{1}$$

$$V_{GS,\,\mathrm{int}} = V_{GS,n} - I_{D,n}R_{S,n} \tag{2}$$

where $R_{SD,n}=R_{S,n}+R_{D,n}$ and $I_{D,n}$ is the drain current. Over years, several efforts have been made by various research groups to model the threshold voltage [28–31] and strain-induced drive current [32–36] of intrinsic (free from S/D series resistance) NS-Si MOSFETs in analytical forms. To frame our algorithms, we are primarily faced with the task of remodeling such parameters taking into account the S/D series resistance, as described in this section.

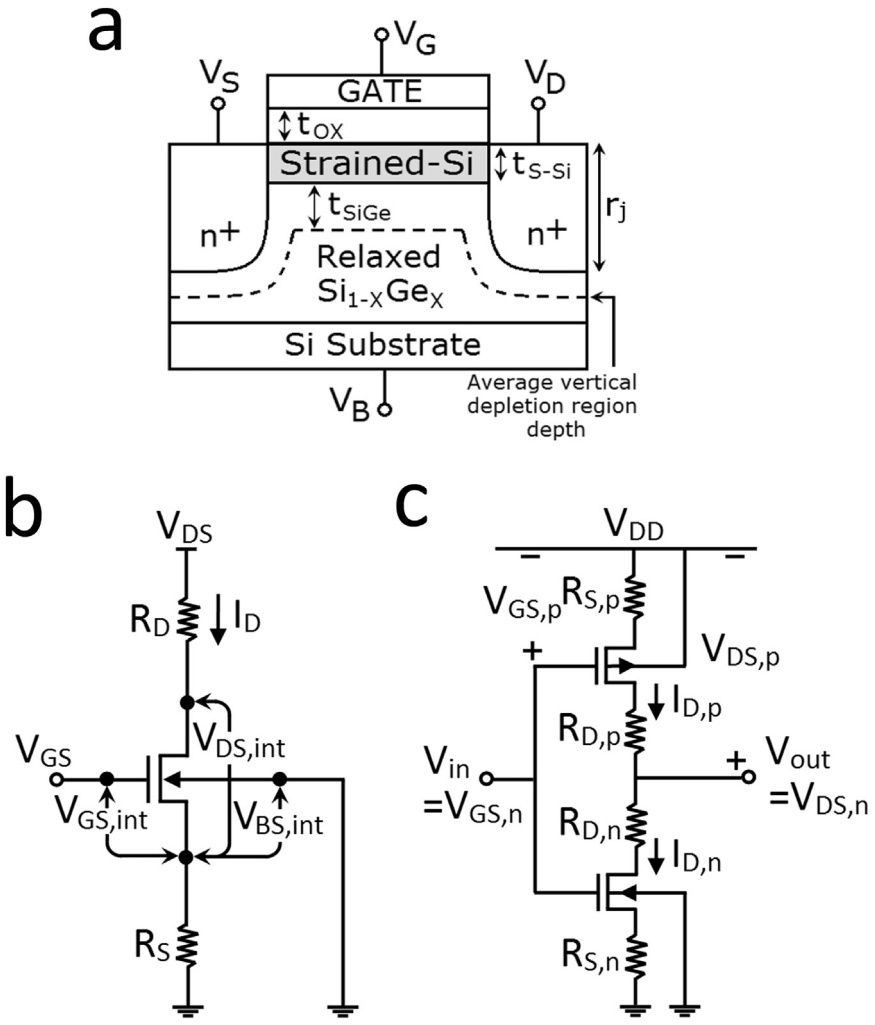

Fig. 1. (a) Generic representation of the cross-section of a n-channel strained-Si/relaxed $Si_{1-x}Ge_x$ MOSFET. (b) Schematic of n-MOS showing source (S) and drain (D) series resistances (R_S and R_D). The intrinsic ('*int*') and extrinsic terminal voltages are also shown. (c) A generalized CMOS inverter incorporating S/D series resistance of n- and p-MOS.