Microelectronics Journal 55 (2016) 19–25

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Oxide thickness and S/D junction depth based variation aware OTA design using underlap FinFET

Ashutosh Nandi [a,*], Ashok K. Saxena [b], S. Dasgupta [b]

[a] Department of Electronics and Communication Engineering, National Institute of Technology Kurukshetra, Kurukshetra 136119, Haryana, India
[b] Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee 247667, Uttarakhand, India

ARTICLE INFO

Article history:
Received 1 September 2015
Received in revised form
25 January 2016
Accepted 31 May 2016

Keywords:
Differential mode gain (A_{DM})
Common mode gain (A_{CM})
Common mode rejection ratio (CMRR)
Electrostatic integrity (*EI*)

ABSTRACT

As the gate lengths of FinFETs are scaled into nano meter regime, spatial variations in oxide thickness (T_{ox}) and junction depth (X_j) of source/drain (S/D) doping profile will largely decide the performance of digital and analog circuits that can fall below or above the desired value. Of particular importance is operational transconductance amplifier (OTA), where the crucial analog figures of merit (FOM) such as differential mode gain (A_{DM}), common mode gain (A_{CM}) and common mode rejection ratio (CMRR) decide the suitability of its use at nanometer regime. In the present work, we have studied the analog performance variation of low-k (dual-k) underlap FinFET based single stage OTA with spatial variation in T_{ox} and X_j of S/D profile. Enhanced and variation less threshold voltage and mobility of dual-k underlap FinFET due to of better screening of longitudinal field and pronounced volume inversion effect, are studied in detail. It is observed that at 16 nm gate length the best case A_{DM}, A_{CM} and CMRR of low-k (dual-k) FinFET based OTA are 34.2 dB (42.3 dB), 26 dB m (18 dB m), 68.2 dB (84.2 dB) respectively. Subsequently, the spatial variation of T_{ox} and X_j leads to worst case change in A_{DM} and A_{CM} of low-k (dual-k) FinFET based OTA by −6.8 dB (−2.2 dB) and +28.2 dB m (+31.3 dB m) respectively. The negligible deterioration in A_{CM} of dual-k FinFET OTA transforms into CMRR improvements of 37% at this worst case condition as compared to CMRR of low-k FinFET OTA. Furthermore, with gate length scaling, the FOM and their percentage change with T_{ox} and X_j of dual-k FinFET OTA are much better than that of low-k FinFET OTA.

1. Introduction

Subthreshold and weak inversion regime of operation of FinFETs are becoming major concern to device designer these days, in order to address the fast growing, wide-spreading application of battery operated portable gadgets such as GSM/EDGE baseband processors for cellular phones, medical instruments, wireless sensor networks, ambient intelligent systems etc. Exponential dependence of channel current on gate potential results in high intrinsic gain and moderate performance that are some attractive features of FinFET, making it a viable alternative to circuit designer in the field of these low power portable applications. For most of the aforementioned applications, the basic analog building blocks are reference circuits, current mirrors, operational transconductance amplifiers (OTA) etc. that are realized using FinFETs. However, as the FinFETs are scaled into smaller process nodes, variations in critical transistor attributes are becoming biggest concern resulting in performance deterioration and aggravated short channel effects. Most importantly, variations in oxide thickness (T_{ox}) and junction depth (X_j) of lateral source/drain (S/D) doping profile are becoming major threats in transistor design as the feature size approaches fundamental dimensions such as the size of atoms and the wavelength of usable light for patterning lithography masks [1,2]. Of particular importance are analog circuits, where resulted device level performance variation can render specification of the particular circuit to fall below or rise above the desired value [3].

Local variations in threshold voltage (V_{th}) and mobility (μ), with process induced variations in T_{ox} and X_j, are two important aspect of analog circuit design at smaller processing nodes [4–6]. The combined effect of V_{th} and μ will deteriorate the transconductance factor $\mu C_{ox}(W/L)$ and subsequently affect transconductance (g_m), output conductance (g_{ds}), transconductance-to-current ratio (g_m/I_{ds}) and intrinsic dc gain (A_{V0}) at device level. This would translate into large variations in crucial circuit level figures of merit (FOM) such as: differential mode gain (A_{DM}), common mode gain (A_{CM}) and common mode rejection ratio (CMRR) [7–10]. More so, the circuit level variations will be pronounced at smaller technology node, if

* Corresponding author.
E-mail addresses: ashutosh.chl@gmail.com (A. Nandi), kumarfec@iitr.ernet.in (A.K. Saxena), sudebdg@gmail.com (S. Dasgupta).

http://dx.doi.org/10.1016/j.mejo.2016.05.014
0026-2692/

the variations in V_{th} and μ are not controlled at device level.

Designing underlap FinFETs with better gate electrostatic control over the channel region can be a possible solution in order to alleviate the ever increasing issues of performance fluctuation at smaller processing nodes. In this regard, dual-k spacer based underlap FinFET is emerging as a strong contender, because of better screening of virtually normal fringing field via inner high-k spacer, thereby controlling the lateral S/D electric field spread into the channel region. This in turn controls direct source to drain tunneling (DSDT), improves short channel effect (SCE) and digital/analog performance [11–14]. The effective screening of dominant fringing field is enhanced with gate length scaling, resulting in improved conduction band energy (CBE) and in turn better threshold voltage and channel carrier mobility [13,14].

Rest of the manuscript is arranged as follows: Section II of the manuscript deals with device structure, specifications and simulation method used. Variation study of V_{th} and μ with local variations of T_{ox} and X_j are analysed in section III which is further extended to circuit performance study. Subsequently, section III A and B analyze the circuit performance of underlap FinFET based single stage OTA with local variations of T_{ox} and X_j. Section IV gives insight into OTA performance study with gate length scaling and the effect of subsequent local variations in T_{ox} and X_j. Finally, section V concludes the paper.

2. Device structure and simulation setup

Fig. 1(a) shows a 3-D underlap FinFET with following specifications: channel doping (N_a)=10^{16} cm^{-3}, peak of doping profile (N_{sd})=10^{20} cm^{-3}, gate length (L_g)=16 nm (except in section IV where it is varied from 16 nm to 12 nm), SOI layer thickness=150 nm. S/D doping profile has been modeled as $N(x)=N_{sd}\exp(-x^2/2\sigma_L^2)$ [15] where, σ_L is the lateral straggle (σ_L) of the dopant species. Subsequently, the junction depth (X_j) is the lateral distance x when the S/D doping profile reaches the channel doping

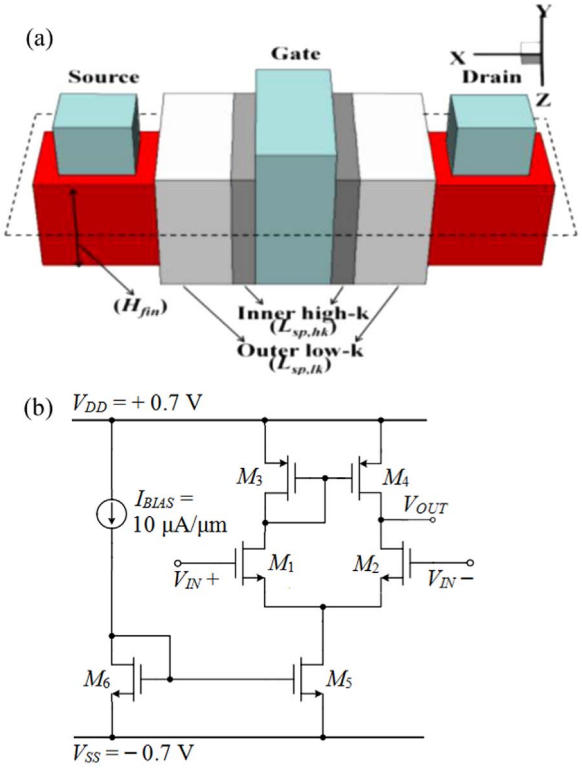

Fig. 1. (a) 3-D Schematic of underlap Dual-k FinFET (b) Single stage OTA circuit.

via suitable value of σ_L. SiO_2 is used as gate oxide throughout the analysis. For conventional low-k FinFET the spacer extension length ($L_{ext}=L_{sp,lk}$) is optimized to 24 nm ($L_{ext}=1.5\times L_g$) [13]. Same optimized spacer extension length ($L_{ext}=L_{sp,lk}+L_{sp,hk}$) of 24 nm and $L_{sp,hk}=L_{ext}/6$ has been used for analysis of dual-k spacer based underlap FinFET [12,13]. SiO_2 is used as single low-k spacer ($L_{sp,lk}$) dielectric for low-k FinFET, whereas TiO_2 (k=40) as high-k inner spacer ($L_{sp,hk}$) and SiO_2 as outer spacer ($L_{sp,lk}$) are used in dual-k spacer based N-FinFET structures [11]. The fin width (W_{fin}) has been selected as 8 nm whereas, aspect ratio (AR) defined as the ratio of fin height (H_{fin}) and fin width, is selected as 5.

Fig. 1(b) shows a single stage OTA that has been designed using conventional and dual-k underlap FinFET at 10 μA/μm of bias current. The 3D mixed mode circuit simulation is carried out using TCAD mixed-mode Sentaurus device simulator including fin depended parasitics calculated from [16] and [17]. Non stationary effects such as velocity overshoot, is introduced by selecting suitable saturation velocity and empirical parameter β as per [18] and [19], to correctly couple the carrier transport phenomena at nanometer regime. Secondly, the impact ionization has been introduced by activating okuto-crowell model and carrier temperature dependent impact ionization model. Furthermore, MLDA quantization model, lombardi mobility model, SRH recombination/generation model, band to band auger recombination and old slotboom bandgap narrowing phenomenon are also included in simulation setup [15]. Metal gate work functions of N-FinFET and P-FinFET are tuned to match the current drive and threshold voltages of the devices. Table 1 list out important attributes that are matched for subsequent analog circuit design.

3. Variation study at 16 nm gate length

Ever increasing demand of miniaturized battery operated portable devices, lead to scaling down the semiconductor device dimensions into nano-meter regime. However, problems like SCE and performance deterioration are crucial issues that are needed to be addressed at device level in order to target optimum circuit performance. Most important is the fluctuation in performance of analog circuits due to local variations in critical transistor attributes such as T_{ox} and X_j. Threshold voltage (V_{th}) and mobility (μ) are two important aspect of device design that are affected due to process induced variations in T_{ox} and X_j. Variation in oxide thickness is a lithography step generated limiting factor at nano-scale devices with shrinking device dimensions [1,20]. Whereas, formation of ultra shallow junction (USJ) is governed by defect formation and junction leakage, temperature control, equipment maturity, process control, cost effectiveness etc. More so, USJ formation is even more difficult in case of P-FinFET because of annealed limited transient enhanced diffusion (TED) in boron [21–24]. Evidently, fluctuation in T_{ox} and X_j are pronounced at lower technology nodes.

Dual-k spacer architecture in underlap section of FinFET will

Table 1
Device specifications.

Attributes	Low-k		Dual-k	
	N-FinFET	P-FinFET	N-FinFET	P-FinFET
σ_L	2 nm	2 nm	2 nm	2 nm
T_{ox}	1 nm	1 nm	1 nm	1 nm
Φ_m	4.69	4.61	4.69	4.61
V_{th}	0.3861	−0.3790	0.4146	−0.4038
I_{OFF}	10 pA/μm	12 pA/μm	2.6 pA/μm	2.1 pA/μm
10 μA/μm @V_{GS}=	0.4516 V	−0.4508 V	0.4762	−0.4719 V