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# Memristor based circuit design using charge and attached capacitor

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ABSTRACT

Memristor is a non-linear circuit element with unique behavior. Specifications of this device complicate memristor based circuit design. Ideal memristor is the function of total applied charge so it can be expressed and controlled in terms of charge only. On the other hand, generic and extended memristors could not be modeled using charge only equations, therefor an extension is required. The aim of this paper is to introduce a new memristive circuit design approach based on charge and attached capacitor. The main benefit of this approach is to change the rule of time from a design parameter into a design condition. Our approach is based on instantaneous charging and branching of an attached capacitor with target memristor. Among known memristors, RRAM is used in this work thanks to its emergent properties and well investigated theory and models. Two RRAM models are used in this paper, which can be grouped into two classes of ideal generic and extended memristors. The ideal generic based model is not realistic but is used to explain the design concept. The proposed methodology is applied to design new memristor based digital to analog converters. During our work, we developed some additional blocks, which can be used in other analog applications. The circuit level simulations are performed using SPICE to evaluate design approaches.

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## 1. Introduction

Theoretically, memristor was personated as a passive two terminal circuit element in 1971 by L.Chua [1]. Memristor is a non-linear circuit element with hysteresis loop, which is pinched at the origin and increasing the frequency turns hysteresis loop into a single-valued function [2]. Memristor as an emerging technology with computation and storage capabilities has been used in imply logic based digital operations [3], in memory computation [4], more complex computations like fast Fourier transform [5] and non-volatile memories [6]. One of the common usages of memristor is in artificial intelligence domain [7]. Memristor also has been used in reconfigurable analog circuits as programmable element [8], in analog computations as analog memory [9], in FIR filter as analog timing storage element [10] and in conversions between analog and digital domains as programmable weight [11].

According to Chua's description, memristors could be grouped in four classes as Ideal, Ideal Generic, Generic and Extended Memristors [12]. Spin-transfer Torque Magnetoresistive Memories (STT-MRAM), phase change memories (PCM), conductive bridge memory (CBRAM) and resistive random access memories (RRAM) [13,14] are examples of available physical memristors. These memristors can be described by a specific memristive class.

Among the above-mentioned memristor variants, RRAM is our preferred memristor along this paper. It was selected due to circuit behavioral requirements and well investigated models describing its dynamics. RRAM models are including linear ion drift model [15], nonlinear ion drift model [16], Simmons tunnel barrier model [17] and current and voltage threshold adaptive memristor models [18,19].

Two models, of linear ion drift model [15] and Stanford RRAM model [20] will be used in this paper. The former is the first proposed RRAM model that defines an ideal generic memristor. This model considered to be in agreement with memristor as flux-charge linkage and cannot be used as a practical model. This model was adopted in the proposed design to introduce charge oriented design concept, which our advanced design is established upon that. Advanced approach named attached capacitor based design and uses Stanford RRAM model, which is an extended memristor. To show the application of the proposed approaches, Digital to Analog voltage converters (D2A) has been designed and SPICE simulations confirmed the presented approaches. Due to impracticality of first model there will be no emphases in simulation results of first model. Even though, new D2A design is not target of this paper, but to show the limitations and sensitivity of the proposed approach, we performed several Monte-Carlo simulation for attached capacitor based design using second model.

The paper is organized as follows: Section 2 presents required basic concepts and definitions of interest in this article. In Section 3 charge-oriented design which is applicable to ideal and ideal generic memristors has been introduced following simulation

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results of the proposed digital to analog converter. Section 4 contains attached capacitor based design for extended memristor and the simulation results of designed D2A. Finally in Section 5, a conclusion is given.

## 2. Basic concepts

Symbol and polarity of memristor in this paper is shown in Fig. 1. The thick black line indicates the polarity of device. If current flows from black line side (Fig. 1(a)) the resistance will decrease and opposite direction of current will increase the resistance (Fig. 1(b)).

### 2.1. Linear ion drift memristor model

Equation of this device is shown in (1) [15]. In this equation $R_{ON}$ and $R_{OFF}$ are lowest and highest resistance of device, $D$ is the device length, $\mu_v$ is the average ion mobility and w is the state variable. By comparing this equation to memristor classes it reveals that this model defines an ideal generic memristor.

$$\begin{cases} v(t) = \left(R_{ON}\dfrac{w(t)}{D} + R_{OFF}\left(1 - \dfrac{w(t)}{D}\right)\right)i(t) \\ \dfrac{dw(t)}{dt} = \mu_v \dfrac{R_{ON}}{D} i(t) \end{cases} \tag{1}$$

The $\phi$–$q$ and $R$–$q$ curves of linear ion drift model are shown in Fig. 2. In (2) the equation of state dependent resistance of this model is shown [15]. Memristance of this model can be written as $R(q)=a-bq(t)$, where a and b are constant values. Also this device could be expressed using flux only equations, which is not discussed in this paper [21].

$$R(q) = R_{OFF}\left(1 - \frac{\mu_V R_{ON}}{D^2} q(t)\right) \tag{2}$$

### 2.2. Extended memristor

Based on conduction mechanisms, including Fowler–Nordheim tunneling, trap-assisted tunneling, Poole–Frenkel tunneling, or direct tunneling in RRAMs, several RRAM models use equation in general form as (3) [20,22,23].

$$I \propto \exp(.)\sinh(.) \tag{3}$$

Stanford RRAM model is a well-defined memristor model. In the equations of Stanford RRAM model (4) $g$ is the state variable corresponds to gap length, $I_0$, $g_0$ and $V_0$ are fitting parameters, $E_a$ is the activation energy, $\nu_0$ is the velocity (the attempt-to-escape frequency included), $L$ is the device thickness, $a$ is the hopping site distance, $V$ is the applied voltage, $k$ is Boltzmann constant, $T$ is temperature and $\gamma$ is the local enhancement factor which is a function of gap state.

$$\begin{cases} I(g,V) = I_0 \exp\left(\dfrac{-g}{g_0}\right)\sinh\left(\dfrac{V}{V_0}\right) \\ \dfrac{dg}{dt} = v_0 \exp\left(\dfrac{-E_{a,m}}{kT}\right)\sinh\left(\dfrac{qa\gamma V}{LkT}\right) \end{cases} \tag{4}$$

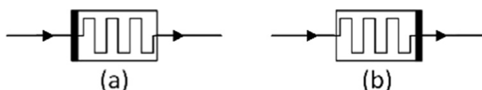


**Fig. 1.** Memristor symbol and polarity; (a) resistance decrease current direction; (b) resistance increase current direction.

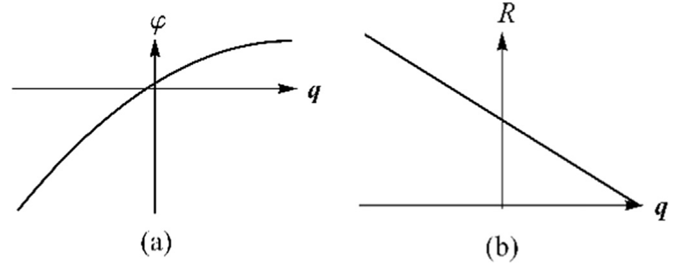


**Fig. 2.** Linear ion drift model Memristor's; (a) $\phi$–$q$ and (b) $R$–$q$ curves.

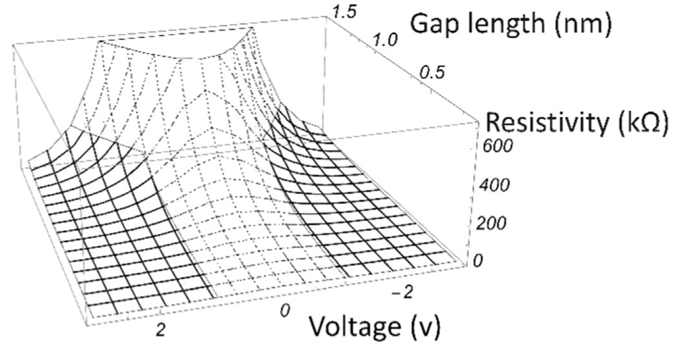


**Fig.3.** Extended memristor resistivity vs voltage and gap status.

If we rewrite the current equation of this model to get the conductivity (5), it reveals that this model defines an extended memristor.

$$G(g,V) = \frac{I_0 \exp\left(\frac{-g}{g_0}\right)\sinh\left(\frac{V}{V_0}\right)}{V} \tag{5}$$

The gap and voltage dependent resistivity of this model is plotted in Fig. 3. There is a parameter in this model as minimum field ($F_{min}$). This parameter defines the minimum required electric field for the movement of ions. In Fig. 3, that portion of surface which marked by dotted mesh is the un-changeable resistivity area according to $F_{min}$.

The absolute value of dynamic Eq. (4) is plotted in Fig. 4(a). There is no limitation on state variable variations in dynamic equation, thereby increasing the applied voltage will cause severe increment in d$g$/d$t$. This extreme increment can cause full state change in one simulation time period, which is incorrect and can lead to logical hazards. This model also has no window function and uses if-else statements instead. To resolve these issues, we added a speed saturation function (6) and a window function (7) to the main model.

The idea of speed saturation function (6) came from electron saturation speed in the electric field, where $V_{sat}$ is the saturation speed of ions, and $\beta$ is a fitting parameter.

$$\begin{cases} \dfrac{dg}{dt} = \dfrac{dgt0}{\left(1 + (dgt0/Vsat)^{\beta}\right)^{\frac{1}{\beta}}} \\ dgt0 = v_0 \exp\left(\dfrac{-E_{a,m}}{kT}\right)\sinh\left(\dfrac{qa\gamma V}{LkT}\right) \end{cases} \tag{6}$$

The Bioleck window function (7) was proposed to consider nonlinear behavior of the linear ion model (1) in the memristor boundaries [16]. The non-linearity and flatness of window function are controlled with parameter $p$. We add this window function to Stanford RRAM model with high value of $p$, which yields a large flat window function to set the dg/dt to zero in memristor boundaries.

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