Microelectronics Journal 55 (2016) 64–69

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A 0.5-V novel complementary current-reused CMOS LNA for 2.4 GHz medical application

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ARTICLE INFO

Article history:
Received 7 August 2015
Received in revised form
16 May 2016
Accepted 24 June 2016

Keywords:
Low voltage
LNA
Modified complementary current-reused
Diode connected MOSFET bias
Forward body-bias
Harmonic rejection

ABSTRACT

A 0.5-V low noise amplifier (LNA) for 2.4 GHz medical application based on 0.18 μm CMOS process is presented in this paper. To achieve low noise and high gain with the constraint of low voltage and low power consumption, a novel modified complementary current-reused LNA using forward body bias technology is proposed. A diode connected MOSFET forward bias technique is employed to minimize the body leakage and improve the noise performance. A notch filter isolator with harmonic rejection is constructed to improve the linearity of low voltage. The measured results show that the proposed LNA achieves a power gain of 18.7 dB and a noise figure of 1.52 dB, while the consuming DC current is only 4.2 mA at supply voltage of 0.5 V.

1. Introduction

With the advance of wireless communication system and technology in recent years, many wireless electronic products such as smart-phone become more portable, power-saving, and also provide a greater variety of services [1–6]. And today with the development of the Internet of things (IoT), wearable devices and medical electronics, the market demand of low voltage low power (LVLP) radio frequency front-end ICs is rapidly growing.

As the downscaling of CMOS process, the high frequency characteristic of MOSFET is improved and suitable for RF and microwave application. Meanwhile the RFCMOS technology is cheaper than the GaAs or BiCMOS technology and can be integrated with base-band circuits [1–10]. At present the widely application of WLAN, RFID, WWAN in medical trade benefit from the development of low-cost wireless CMOS technology [3–9]. To prolong the life of batteries in portable medical devices and systems, low-voltage, low power and low-cost high performance CMOS RF circuits are required. The design of such circuits is therefore a key issue.

Low noise figure, low power consumption, high gain and high linearity of CMOS RF amplifiers such as LNA and PA, are extremely important to wireless communication system. However, it's almost impossible to achieve a strategy which can face all the desired performance, especially in application of low voltage and low power. Some work and technique about low voltage CMOS low noise amplifier are reported, but they seem can not achieve a good trade-off between low voltage, low power and high performance, especially high gain. The current-reused technique is proposed for low power application while preserve high gain. Moreover complementary current-reused technique is proposed for low voltage and low power application, unfortunately its character of preserve high gain is not significant [2–5].

In this paper, a 0.5-V 2.4 GHz novel modified complementary current-reused CMOS LNA with diode connected MOSFET forward body bias technique is designed and realized for the first time in a 0.18 μm RFCMOS technology. The LNA not only demonstrates the feasibility of the design methodology but also achieves the high gain and low voltage performances simultaneously with low power consumptions among previously reported CMOS LNAs. This paper is organized as follows. In Section 2, circuit design and analysis is presented. In Section 3, the measured results and a comparison with other published works are shown. Section 4, summarizes and concludes this work.

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http://dx.doi.org/10.1016/j.mejo.2016.06.011
0026-2692/

2. Circuit design and analysis of the proposed LNA

2.1. Novel architecture of complementary current-reused LVLP LNA

The technique of current-reuse is proposed to reduce the power consumption of LNA while preserving high gain [1–3]. However, the traditional current-reused LNA topology uses a NMOS as the cascaded stage and requires a larger supply voltage to keep saturation operation of transistors. To operate the LNA at reduced supply voltage below 0.8-V with a sufficient gain at multi-gigahertz, a complementary and current-reused architecture is proposed as shown in Fig.1 for low voltage and low power LNA application [2–5]. The amplified RF signal from Mn is impeded by the high reactance of isolation inductor Liso and bypass capacitor Cgnd and directed to the gate node of Mp only via a coupling capacitor Ci. Since the LNA topology is with cascaded amplifier stages, an enhanced gain is achieved in ultra-low-power and ultra-low-voltage designs. Unfortunately its character of preserving high gain is not significant due to inter-stage mismatch. Meanwhile the linearity is restricted by the ultra-low supply voltage and the voltage drop across the parasitic resistance from inductor in the path of Vdd to ground.

To achieve a further enhanced gain and an enhanced linearity in ultra-low-power and ultra-low supply voltage designs, a novel modified complementary current-reused LNA topology with cascaded common source (CS) amplifier stages (input NMOS and output PMOS CS) is proposed, and the complete circuit schematic of the proposed LNA is illustrated in Fig. 2. The transistors Mn and Mp operate in the common source (CS) amplification configuration and they share the same DC bias current flowing through Liso. The amplified RF signal from Mn is impeded by the high reactance of the resonant Liso and directed to the gate node of Mp through the coupling and matching network Li and Ci. The overall trans-conductance is equal to the multiplication of the individual trans-conductance of Mn and Mp.

As for the DC bias under 0.5-V supply voltage, the gate of input NMOS is connected to Vdd through RF resistor R_{bias}, while the gate of output PMOS is tied to the ground through biased and matching inductor L_i. In order to obtain simultaneous power and noise

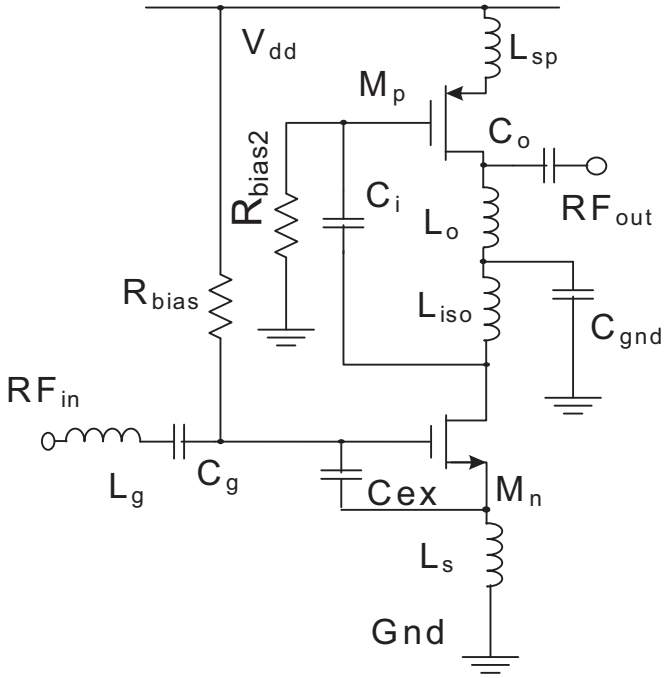

Fig. 1. Conventional current-reused topology.

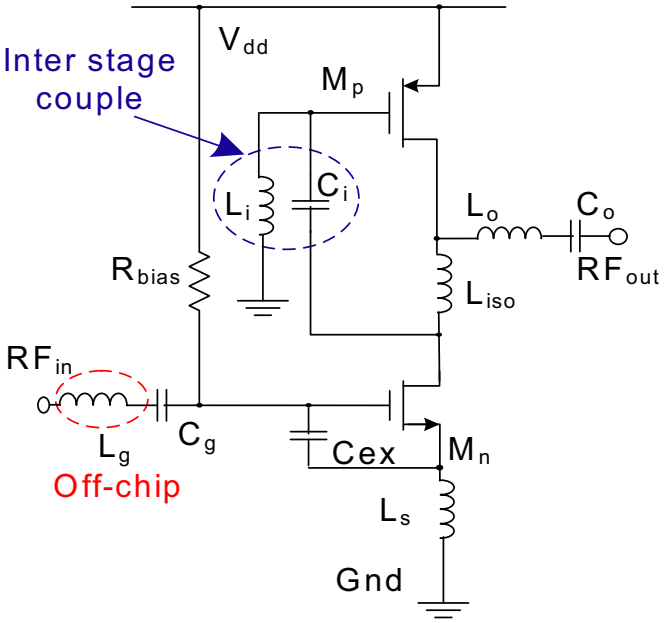

Fig. 2. Novel modified complementary current-reused LNA topology with two cascaded CS gain stages.

matching for the input stage, the inductive source degeneration with Ls, Cex and off-chip inductor Lg is adopted. On the other hand, the output matching is provided by Lo and Co with the parasitic capacitor. Meanwhile a LC-tank (L_i and C_i) network is employed as inter-stage signal coupling and matching for further improve the gain. The gate width of the CS NMOS/PMOS is traded off among power consumption, noise figure, linearity and gain via the optimization of source-drain across voltage.

The circuit schematic of an equivalent two-stage cascaded CS amplifier for Fig. 2 is shown in Fig. 3 Unlike the choke inductor with bypass capacitor in conventional complementary C–R topology, in this design an optimized choke inductor is used for connecting the drain of each common source transistor together. Synthetically with the source/drain parasitic capacitor of the output cascade PMOS, an inter-stage notch filter is constructed as the isolator for inter-stage fundamental signal isolation of current-reused. Note that, under similar bias conditions, the amplifier gain is further enhanced by the cascaded common source PMOS stage with optimized matching and isolation network. Therefore, it has a comparable power gain to the cascaded CS topology.

2.2. Linearity consideration of the novel complementary current-reused LVLP LNA

In traditional C–R with inductor block and bypass capacitor, since all the high frequency output nonlinear power (harmonic

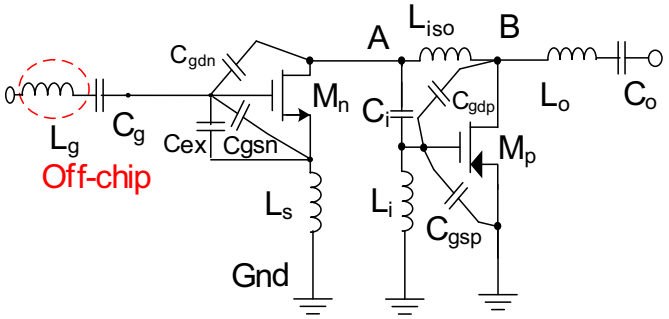

Fig. 3. Circuit schematic of an equivalent two-stage cascaded CS amplifier.