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Performance comparison of conventional and strained FinFET inverters

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ABSTRACT

In this paper, we have investigated the effect of tensile and compressive stress on the performance matrices of complementary FinFET inverters. The static and dynamic characteristics have been compared with conventional Silicon FinFET inverter. Epitaxially grown Silicon–Germanium (SiGe) and Silicon–Carbide (SiC) source/drain (S/D) are used as stressors for p- and n-FinFET, respectively, over Bulk and SOI substrates. Further, the effect of asymmetric doping at source/drain have been analyzed and compared with the symmetric one. It has been found from the transient response that due to strain, the mobility is enhanced across channel and the switching speed has increased. However, for unequal doping, due to unbalanced stress the propagation delay has been enhanced upto 20% in comparison to symmetric inverters. The minimum propagation delay of 45 ns for strained Bulk inverter has been found due to high driving current in FinFETs. The fin shape dependence changes also has been investigated by varying top fin width. Rectangular to triangular fin shapes variation caused reduction in delay of about 10–13%.
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1. Introduction

FinFET is a promising candidate in the categories of innovative architecture for sub 14-nm technology node [1]. Great controllability over channel current with two/three gates and reduction in short channel leakage current are the key aspects for this device [2]. However, ultra low power (ULP) digital integrated circuit (DIC) applications are continuously demanding for high speed and multi-threshold voltage devices. To improve the driving current, strained technology for CMOS is on mass production [3] and is also appreciated for the designing of FinFETs [4]. One of the techniques to enhance the mobility of charge carriers across the channel is Source/Drain (S/D) stressor [5,6,1,7]. Stress across channel can be compressive using Silicon Germanium (SiGe) [1] or tensile using Silicon Carbide (SiC) [8] S/D for PMOS and NMOS, respectively. Hence, it is imperative to find the effectiveness of these stress techniques on circuit performance. Furthermore, stress across the channel also has been influenced by Bulk and SOI substrate [9], thus the driving current and speed of operation also varied by changing the substrate.

Charge carriers in FinFETs depend on the shape of fin and are normalize using effective fin width (W_{eff}), which is a function of top (W_{top}) and bottom (W_{bot}) fin widths. Although, the rectangular fin shapes ($W_{top}=W_{bot}$) are default design for FinFET, but Auth et al. of Intel [10] have introduced fin shape which is almost triangle ($W_{top} < W_{bot}$). Thus, the fin cross section and W_{eff} get changed with modification in W_{top}. W_{eff} is one of the main objective for defining the scaling of FinFET based digital circuits. The fin cross section, maximally affects the On and Off currents and threshold voltage of devices [7,10]. Gaynor et al. [11] found that the leakage current in triangular fin is sufficiently reduced over rectangle fin. Stress is also defined across the cross sectional area of fin, so the mobility of charge carriers also influenced by change in fin shape . Because of this, the driving current of the devices are strongly affected by triangle and rectangle fin shapes for strained FinFETs. Apart from this, asymmetry in device structure also affect the performance of the circuit. While, Moradi et al. proved that due to asymmetric doping across source and drain the performance of SRAM cell can be improved [12], Goel et al. found the performance enhancement of circuit due to different spacer length at both side [13].

In this paper, we have analyzed various aspects of complementary FinFET inverters' performance through simulation using technology computer aided design (TCAD) tool. The analysis has been done in two part, first, the static and dynamic characteristics have been measured and compared for strained and conventional circuits with different fin shapes. Strained inverters have been designed using SiGe and SiC S/D on p- and n-FinFET, respectively. Second, the influences of asymmetric doping at drain and source side, have been examined for all the inverters. The fin shape dependent changes have been considered by changing W_{top}

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Table 1
Devices types for three inverters.

Inverter	Device type	Type of stress	Stressor
Strained Bulk inverter(s-Bulk Inv)	n-FinFET p-FinFET	Tensile Compressive	SiC S/D SiGe S/D
Strained SOI inverter (s-SOI Inv)	n-FinFET p-FinFET	Tensile Compressive	SiC S/D SiGe S/D
Conventional Bulk inverter(c-Inv)	n-FinFET p-FinFET	None None	None None

and asymmetry has been generated by changing the drain side doping (N_{drain}). Hence, the transfer and switching characteristics have been presented for inverters designed by (a) Bulk FinFETs with S/D stressor (s-Bulk FinFET) , (b) SOI FinFETs with S/D stressor (s-SOI FinFET) and (c) Conventional Bulk FinFETs with Silicon S/D (c-FinFET), as described in Table 1. Section 2, described the design approach used for n- and p-FinFET devices. In Section 3, the static and dynamic performance matrices have been compared. Finally, the conclusions are covered under Section 4.

2. Simulation approach

Design of Bulk and SOI devices have been done using Sentaurus TCAD provided by Synopsys [14], and followed the process steps of [9]. Device features are shown in Table 2 and opted according to international technology road map for semiconductor (ITRS-2013) [15]. Process simulator under Sentaurus has been adopted for the design of n-and p-FinFETs on different wafers. For compressive stress across channel, source/drain stressors; Carbon doped Si : $Si_{1-y}C_y$ for n channel FinFET [16] and Si-Germanium: $Si_{(1-x)}Ge_x$ for p channel FinFET are used. Stress effects have been introduced by dealing with Ge mole fraction (x) of 0.5 and C mole fraction (y) of 0.02.

The devices were designed on Bulk and SOI substrate with (100) orientation and channel direction of (110). Possible processing steps for strained Bulk FinFET are: (a) Fin pattering (For etching of triangular fin the procedure used by N. Lindert et al. in [17], can be used) (b) gate oxide deposition (c) poly gate deposition (d) spacer formation (e) selective epitaxial growth of SiC and SiGe source and drain at 600 °C for n- and p-FinFET, respectively (f) poly gate removal and metal gate deposition (g) contact deposition . For SOI FinFET, Si is etched across the active area prior to epitaxy of S/D, rest steps are same as given above. The gate-last technique has been used for metal gate stack formation, with midgap work function of Tungsten [18] on HfO_2 for both n- and p- channel FinFET. Conventional Bulk FinFET follows the exact processing steps that have been used above, except the S/D are of Si. Complete architecture of the device for both Bulk and SOI substrates are shown in Fig. 1(a and b).

Inverter performance analysis has been done through mixed mode simulation under the device simulator of Sentaurus [19]. Drift diffusion model is used to account the charge transport across the channel. Philips unified mobility and high-field mobility saturation model is used to calibrate electron and hole mobility in FinFET. Quantum separation due to carrier mass density-gradient has been found by quantum correction model, and it based on Poisson–Schrodinger equation. Lattice mismatch deformation between Si–Ge and Si–C is calibrated using the stress-dependent deformation of band structure model. Consideration of band structure deformation, which is caused by stress, has done through two-band k.p and six band k.p models for electrons and holes, respectively. Quantum mechanical model to get the density of electrons and holes under stress, has been activate by modified local-density approximation (MLDA). Further, the circuit simulation has been done through multidevice analysis under mixed mode simulation, for the transient and DC performance.

3. Inverter performance analysis

3.1. Symmetric S/D doped strained inverters

3.1.1. Voltage transfer characteristic (VTC)

Voltage transfer characteristics (VTC) is the figure of merit for static behavior of inverters, which is defined by V_{out} as a function of V_{in}, and depends on the driving current of pull up and pull down transistors. However, variations in On and Off currents and threshold voltage (V_{th}) have occurred for different fin shapes. It is due to change in charge carrier distribution and stress across channel. In this work, we have used rectangle and triangle fin shapes as shown in Fig. 2(a and b) for conventional and strained FinFET, and accordingly evaluate the performance for the inverters. For this section, doping at source and drain are equal ($N_{drain}=N_{source}$), and the devices are referred as symmetric.

With supply voltage of 0.8 V, the VTC for inverters are shown in Fig. 3 (a and b). Here, VTC of conventional and strained FinFETs are compared for $W_{top}=5$ and 10 nm. S/D stressors enhance the mobility of charge carriers across the channel, which improves the pull up and pull down currents of inverters. s-Bulk Inv gives the steep transition at input voltage of $V_{DD}/2$, while for c-Inv, it is at 0.45 V. For $W_{top}=5$ nm, due to deviation in threshold voltage and driving currents, VTC for s-SOI Inv moves towards the ideal behavior whereas degrades for conventional one. Gain plot for all the inverters ($\partial V_{out}/\partial V_{in}$) are shown in Fig. 3 (c and d). Highest gain of 23 dB has been found for c-Inv with voltage shift of approx 3–5 mV from the transition point. s-SOI Inv has a gain of 22 dB at the transition point i.e.$V_{DD}/2$.

Table 2
Device dimensions.

Parameter	Dimensions
Fin height (H_{fin})	24 nm
Fin Width	$W_{top}=W_{bot}=10$ nm $W_{top}=10$ nm , $W_{bot}=5$ nm
BOX/STI thickness	40 nm
Gate length (L_g)	17 nm
Spacer length (L_{spa})	16 nm
Oxide thickness (T_{ox})	2.9 nm
Source doping concentration(N_{source})	$2\times10^{18}(cm^{-3})$
Drain doping concentration (N_{drain})	$2\times10^{18}(cm^{-3})/1\times10^{18}(cm^{-3})/1\times10^{17}(cm^{-3})/5\times10^{17}(cm^{-3})$
Channel doping concentration	$2\times10^{15}(cm^{-3})$

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