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Physical design of quantum circuits in ion trap technology – A survey

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A B S T R A C T

Quantum circuits have indicated incredible potential for having the capacity to take care of specific issues, which are unmanageable on classical machines. Research in quantum circuit design distinguishes between logic synthesis and physical design. In this survey, we review the approaches, exact and heuristic, proposed for physical design automation of quantum circuits in ion-trap technology that is one of the most advanced quantum technologies. We finish up the review by sketching out major open problems for quantum circuit design.

1. Introduction

As feature sizes in CMOS[1] technology shrink into the 10s of nanometer range, “quantum effects” should be managed [1]. On the other hand, quantum effects such as superposition and entanglement are amplified and utilized in a quantum computer. Quantum circuits will have the capacity to solve some important mathematics and physics problems with fascinating asymptotic improvements [2–5]. A quantum computer needs a large number of qubits and quantum gates to tackle a complex job such as factoring large numbers. To manage the complexity of the big systems, researchers divide the design flow into two main processes: logic synthesis and physical design. The logic synthesis process takes a design description as input and creates a technology-dependent gate-level netlist as output. On the other hand, the physical design process takes the output of the synthesis process and generates a specific layout constructed from the building blocks of the target technology.

The finding of effective quantum algorithms in the mid-1990s [6] and remarkable progress in quantum technologies motivate research on physical design. Extensive research has concentrated on finding physical systems that can provide a large number of qubits while satisfying the scalability criteria [6]. Ion traps have been the physical system of choice [7] to demonstrate the most advanced quantum logic operations [8–13]. A preliminary architecture has been proposed for assembling a large number of ions into a multiplexed trap on a chip [14]. Much research has been done on the physical design of quantum circuits in ion trap technology. This review talks about methodologies, architectures, optimization techniques, open issues, and future directions related to the physical design of quantum circuits in ion trap technology.

Some papers presented physical principles of ion traps such as specific electrode sizing and geometry, and exact voltage levels necessary for trapping and movement, and technology choices for building a large-scale ion trap quantum information processor (QIP) such as which ion species are used [14–20]. The main concentration of those papers is on the physical requirements of such a system. Such papers about the physics of the ion trap technology are not the purpose of this paper. This paper mainly focuses on the methods proposed for automation of the quantum circuit physical design in ion trap technology. The papers discussed in this survey use an abstract model of ion trap technology. They encapsulate all physical details within some building blocks.

A few works were performed on the physical design in other technologies. In research performed by Maslov et al. [21], an efficient heuristic algorithm was proposed for quantum circuit placement in the NMR[2] technology. In the other work, Shafaei et al. [22] formulated the qubit placement on 2D optical lattice by mixed integer programming. Lin et al. [23] proposed a physical design-

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[1] Complementary metal oxide semiconductor.

[2] Nuclear magnetic resonance.

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aware quantum circuit synthesis methodology in the optical lattice technology, called PAQCS[3], that includes two algorithms for qubit placement and channel routing.

The rest of this paper is organized as follows: basic concepts are presented in Section 2, followed by an introduction to the ion trap technology in Section 3. Section 4 includes the design flow for quantum circuits. Moreover, works on the physical design are described in that section. Software tools developed for the physical design are presented in Section 5. Finally, Section 6 concludes the paper, and gives the future directions and open problems in quantum circuit design.

2. Background

In this section, quantum bit, quantum logic gates, and quantum circuits are introduced. Some basic concepts that can be helpful in understanding the rest of the paper, are also mentioned.

2.1. Quantum bit (Qubit)

The bit is the key concept of classical computation and information. Quantum information processing is based upon an analogous concept, the quantum bit, or qubit for short [24]. In fact, a qubit is a unit vector in a two-dimensional Hilbert space. The state of a qubit, $|\psi\rangle \in H^2$, can be represented using the canonical base $|0\rangle$ and $|1\rangle$ as

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle, \qquad |\alpha|^2 + |\beta|^2 = 1,$$

Therein, the numbers α and β are complex numbers. These linear combinations of states are often called superposition. The special states $|0\rangle = \begin{pmatrix}1\\0\end{pmatrix}$ and $|1\rangle = \begin{pmatrix}0\\1\end{pmatrix}$ are known as computational basis states, and form an orthonormal basis for the vector space. What the vectors $|0\rangle$and $|1\rangle$ physically mean depends on the physical demonstration used for quantum-information processing. For example, the vectors may represent spin states of an electron, $|0\rangle = |\uparrow\rangle$and $|1\rangle = |\downarrow\rangle$. Electrons are replaced by nuclei with spin $\frac{1}{2}$ in NMR quantum technology [25].

2.1.1. Physical qubit

In ion trap technology, a physical qubit is represented by a single positively charged ion.

2.1.2. Logical qubit

A logical qubit is a bit of data used in the computation. It may be physically encoded in some number of physical qubits.

2.1.3. Ancilla qubit

Ancillae are helper qubits used in quantum computation. They include qubits that are created, used, and recycled as a part of a computation. The main usage of these qubits is in quantum error detection/correction algorithms.

2.1.4. Quantum register

An ordered set of a finite number of qubits is called a quantum register.

2.2. Quantum gate

An n-qubit quantum gate is an operator which performs a $2^n \times 2^n$ unitary operation $\mathbf{G}$ on n qubits in a particular period of time. A matrix $\mathbf{G}$ is unitary if $\mathbf{G}\mathbf{G}^{\dagger} = \mathbf{I}$ where $\mathbf{G}^{\dagger}$is the conjugate transpose of $\mathbf{G}$ and $\mathbf{I}$ is the identity matrix. The number of input qubits of a quantum gate should be equal to the number of its output qubits. The inverse of a quantum gate g with a unitary matrix $\mathbf{G_g}$ shown by g^{-1} implements the unitary matrix $\mathbf{G_g^{-1}}$. Unitary operators are often represented by particular schematic symbols, which are useful in the quantum circuit design. Basic quantum gates are shown in Fig. 1. A group of multi-qubit logic gates is the controlled-U gates. These gates have some control qubits and a target qubit. If all control qubits are set to 1, the unitary matrix $\mathbf{U}$ is applied to the target qubit. The set of reversible gates whose matrix elements are just 0s and 1s is part of the set of quantum gates [26].

Quantum wires connect gates together and move qubits forward in time or space. A quantum bit with unknown state cannot be cloned; therefore, quantum wires cannot fanout. Matrix multiplication and tensor product are used to model composition of gates in series and in parallel respectively.

2.2.1. Macro gate

A macro gate has more than three inputs. For example, a C^4NOT that has four control lines and one target line is known as a macro gate [27].

2.2.2. Auxiliary qubit

An auxiliary qubit is a qubit that is not in the set of primary inputs of a macro gate but used to decompose the macro gate into primitive gates. The main feature of auxiliary qubits is that their values before and after a macro gate are equal [6].

2.3. Quantum circuit

The quantum circuit can be used as a computational model similar to a modern digital circuit to represent a quantum algorithm. A quantum circuit comprises of qubits, quantum gates, quantum wires, and qubit measurements. The quantum circuit for a 4-bit Quantum Fourier Transform (QFT) is shown in Fig. 2, which includes the Hadamard and controlled phase shift gates. In quantum circuit model, time goes from left to right and each line shows the evolution of each qubit through time. If each gate in a quantum circuit is inverted and the order of gates is reversed, the inverse of the circuit will be constructed. All quantum operations in a quantum circuit are reversible, except for measurements that are often deferred to the end of computation.

2.3.1. Universal set of gates

A universal set of quantum gates is a set of gates that any unitary operation may be implemented to arbitrary precision by a circuit, including only those gates [6]. For example, Hadamard, phase, CNOT, and $\frac{\pi}{8}$ gates make a universal set.

2.3.2. Stabilizer circuits and states

Stabilizer circuits are a valued subclass of quantum circuits, which can be simulated on classical computers efficiently in polynomial-time and by keeping track of the Pauli operators that stabilize the quantum state. Such stabilizer operators are kept up during simulation and uniquely show stabilizer states up to an unobservable global phase factor. Therefore, this technique offers an exponential improvement over the computational resources needed to simulate stabilizer circuits using vector-based representations. Most research [6,29–31] has been done on stabilizer circuits because of their broad applications in quantum error correcting codes and quantum fault-tolerant architectures.

2.3.3. Quantum threshold theorem

One of the most important theorems in the quantum computation is quantum threshold one [32]. It states that an arbitrarily

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[3] Physical design-aware fault-tolerant quantum circuit synthesis.