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A scalable voltage controlled oscillator for multi-rate high-speed interfaces

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ABSTRACT

This paper proposes a voltage controlled oscillator (VCO) which is based on a pseudo-differential ring oscillator suitable for multi-Gbps serial interfaces. The delay element employed in the ring oscillator topology consists of two CMOS inverters loaded by a simple negative resistance realized with pMOS transistors. The proposed topology is designed and simulated in a 65 nm CMOS process with 1.2 V supply voltage. As a realistic application, the VCO performance is optimized to be compliant with the MIPI Alliance M-PHY standard which is the most updated high-speed serial interface technology. The frequency tuning range covers the three frequency bands of the MPHY standard which are [0.624 and 0.7288] GHz, [1.248 and 1.4576] GHz and [2.496 and 2.9152] GHz and corresponds to high-speed gear 1,2 and 3, respectively. In each gear an almost constant K_{VCO} is achieved while the current consumption of the whole system is 2.87, 5.19 and 10.06 mA for the gears 1,2 and 3, respectively. The phase noise is about −94 dBc/Hz at 1 MHz frequency offset for 2.9152 GHz.

1. Introduction

VCO are basic blocks in almost every electronic circuit which transmits, receives, or processes data. LC VCOs were used until recently for high frequency applications in the range of several tens of GHz. Although they offer excellent performance in high frequency, they need on-chip inductors, requiring a large area on the die. As the pure CMOS processes scales down, ring oscillators (RO) are able to replace LC VCOs for applications above 10 GHz, needing only small area and being comparable in terms of phase noise, power consumption and frequency tuning range. Main applications in which they can be employed are the phase locked loops (PLL) and in most recent state-of-the-art high speed multi-rates serial interfaces clock and data recovery (CDR) [1–8].

In multi-Gigabit systems, a number of non-overlapped frequency bands are normally needed to support different data rates. A power hungry technique can use a single VCO with wide frequency tuning range for multi-Gbps operation. Another solution is to utilize a number of scalable VCOs, each one optimized in terms of performance and area, in order to cover the specified frequency bands. In this solution, the RO is the best candidate because of its small chip area and simple design optimization.

Both single-ended and differential ROs can be used in PLLs. Differential topologies are more suitable for high-speed serial interfaces because they offer better common-mode and power supply rejection performance. However, pseudo-differential configurations [9] are even more suitable for such applications compared with their fully-differential counterparts [10] mainly due to low-voltage operation capability, small chip area, high voltage swing and reasonable low phase-noise performance with a relatively small current dissipation [11,12]. There are many pseudo-differential RO design techniques with emphasis on minimizing the phase noise, increasing the oscillation frequency and the tuning range but with the cost of increasing the power consumption [13].

The fundamental topology of an active CMOS RO is an unstable negative feedback loop which comprises an odd number N of identical delay elements (DE) [9]. Due to the unstable condition, the circuit oscillates with a time delay T_D between consecutive DE yielding an oscillation frequency f_o which is given by $f_o = 1/2N \cdot T_D$. The time delay mainly depends on the current drive capability of the DE, the parasitic capacitance C_{par} of DE's output nodes and the wiring parasitic.

There are several published DE in the literature; each of them has different time delay tuning methodology with pros and cons.

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A tuning technique uses a simple controllable latch in order to implement a positive feedback loop and to ensure oscillation, but it suffers from a dead zone of the input-output response resulting in degraded duty cycle [14]. Other method employs a controllable current source to adjust the small signal transconductance of the DE suffering from non-linear f_o to tuning voltage V_{CTRL} relation [15]. An alternative flexible method uses current-starved inverters, but needs extra circuitry to improve the supply voltage sensitivity [16]. Finally, a smart method employs active inductors to tune out the parasitic and to control the time delay but it suffers from bad phase noise and poor quality factor [17].

A VCO topology for multi-frequency bands applications based on a novel DE is proposed in this paper. The VCO topology utilizes multiple scalable configurations, each one of them is optimized in terms of power consumption and phase noise, covering a wide frequency range from 0.624 GHz to 2.9152 GHz. The VCO is based on a novel pseudo-differential DE which employs two CMOS inverters loaded by a negative resistance formed by a pair of cross connected pMOS transistors [18]. This DE offers an almost linear f_o -V_{CTRL} relation, extended frequency tuning range with almost constant K_{VCO} for reasonable power consumption. The time delay and, therefore, f_o is tuned from an internal supply voltage on the RO which modifies directly the current drive strength of each DE. The VCO performance was optimized in order to be compliant with MIPI Alliance M-PHY specification which is the most updated industrial standard that defines the link for high-speed multi-Gbps short range wire-line applications [8]. The circuit and its layout are designed, simulated and optimized using TSMC 65 nm CMOS process. In Section 2, the VCO system overview along with the top level circuit specifications are presented. In Section 3, the sub-circuit topologies are presented and analyzed. The mathematical derivation of the oscillation frequency versus tuning voltage is presented in Section 4. Finally, in Section 5 the post-layout simulation and comparison results are discussed.

2. VCO system and top level specifications

The M-PHY's standard is addressed to mobile devices and therefore low supply voltage, low power consumption, small chip area and multi-rate data interfaces are among the most important electrical specifications. There are two main modes of rates, the low speed and the high speed. The high speed mode utilizes three main data rates or gears, with two rates for each gear (rate A and B), namely $HS1_{A/B}$, $HS2_{A/B}$ and $HS3_{A/B}$. The gears correspond, as depicted in Table 1, to $HS1_{A/B}$=1.248/1.4576 Gbps, $HS2_{A/B}$=2.496/2.9152 Gbps and $HS3_{A/B}$=4.992/5.8304 Gbps. Assuming that the CDR is based on a half-rate architecture for minimizing the power consumption, the required clock frequencies are $f_{HS1A/B}$=0.624/0.7288 GHz, $f_{HS2A/B}$=1.248/1.4576 GHz and $f_{HS3A/B}$=2.496/2.9152 GHz which correspond to HS1, HS2 and HS3, respectively. The standard also, suggests that a fast locking CDR must recover the phase of the received data within a short synchronization length, employing a small number of clock periods with poor clocks' edge density. A fast locking CDR loop employs a number of internally generated discrete clock phases and selecting the closest one to the received data phase. Therefore, a fast and accurate phase interpolator (PI) with multi phase clock must be available in the loop of CDR. More input phases in PI generate more accurate output phases. These input phases are coming from a multi-stage VCO. On the other hand a ring oscillator with a large number of stages is not able to oscillate in very high frequency. Therefore, the number of the VCO stages is a trade-off between the VCO frequency and the minimum number of the required phases. In a CMOS 65 nm technology, a high frequency differential VCO with 4 stages and 8 clock phases can reach frequency higher than 3 GHz.

Table 1
Gears and rates supported by M-PHY standard.

Gears	Units	Rate A	Rate B
HS1	Gbps	1.248	1.4576
HS2		2.496	2.9152
HS3		4.992	5.8304

The VCO must operate in three gears, according to data rates shown in Table 1. A common method in cases with multiple frequencies is to employ one VCO with a large tuning range covering from the lowest to the highest frequency range, including an overhead for worst process, temperature and bias variations. Depending on the specific delay elements of a ring oscillator, this can be implemented by a large bias voltage or current changes. However, an employment of selective RO can be used, as shown in Fig. 1, to improve performance in terms of power consumption and phase noise. Since the chip area of a RO based VCO is expected to be small, the proposed system utilizes three VCOs; each one of them will be optimized for a specific gear. A 2-bit control word $<gear>$ activates only one VCO which corresponds to the required frequency $f_{HSxA/B}$ where x=1, 2, 3.

Fig. 1 shows the block diagram of the presented VCO, which includes the core block of the 4-stage RO consisted of four identical delay elements and all the necessary sub-circuits such as level shifters, common-mode stabilizers and output buffers/MUX. The 4-stage RO is supplied by a low-drop-out (LDO) regulator, for better low voltage operation capability allowing, also, an extended frequency range without area penalty [19]. The supporting circuits are shared among the three VCOs.

Level shifters (LS) are used to convert the low signal swing which is generated by the 4-stage RO to a rail-to-rail signal swing which drive the next stages [20]. In addition, the common-mode stabilizers (CMS) are used after level shifters stabilizing the output common-mode voltage level around $V_{DD}/2$ over PVT corners [21] and correcting in this manner the duty cycle. Finally, the output buffers/MUX are employed to improve the fan out capabilities of the VCO and select the VCO output for a specified gear.

The used TSMC 65 nm CMOS process offers two flavors of MOS device; the core and the input/output (I/O) MOS devices. The core MOS devices offer lower parasitic, lower threshold voltages and good current factor but they allow lower maximum drain-source and gate-source voltages $V_{MAX.core}$ for reliable performance; $V_{MAX.core}$ for core devices is about 1V. The I/O MOS devices present larger parasitic and threshold voltage but allow higher $V_{MAX.I/O}$. In the proposed design core MOS transistors will be employed in sub-circuits that handle high-frequency signals and the applied V_{MAX} is low enough. On the other hand, the I/O MOS devices will be used in baseband parts, like the LDO, where higher supply voltage is necessary to keep the performance of the VCO improved.

3. Sub-circuit topologies

3.1. Proposed delay element

The proposed delay element, shown in Fig. 2, consists of two CMOS inverters $M_{n1+/-}-M_{p2+/-}$ and a negative resistance formed by a pMOS transistor pair $M_{p1+/-}$. The oscillation frequency f_o tuning is achieved through the supply terminal $V_{DD.RO}$. According to the block diagram of Fig. 1, the $V_{DD.RO}$ is connected to V_{CTRL}. Therefore, V_{CTRL} follows V_{TUNE} changes; both common-mode voltage V_{CM} and output voltage swing will depend on V_{CTRL}. Therefore, a level shifter is necessary to enhance the voltage swing