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Impact of carrier quantum confinement on the short channel effects of double-gate silicon-on-insulator FINFETs

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ABSTRACT

In this work, we use a center potential based approach to determine the electrostatics viz. threshold voltage (V_{th}), Sub-Threshold Slope and Drain Induced Barrier Lowering (DIBL) for Fully Depleted (FD) Undoped Symmetric Double-Gate (DG) Silicon-on-Insulator (SOI) FINFETs over a wide range of Channel Lengths (L_g) and drain voltages (V_d). Based on this approach, a comparison of the electrostatics of Undoped Symmetric Double-Gate (DG) Silicon-on-Insulator (SOI) FINFETs is presented between the semi-classical and quantum confinement cases for two different SOI fin thicknesses of $T_{fin}=2$ nm and $T_{fin}=7$ nm, respectively. For both cases, it is observed that the threshold voltage roll-off and DIBL is greater in the quantum confinement case than in the semi-classical case. This seemingly counter-intuitive trend also implies that the channel length corresponding to the transition from long channel to short channel behavior (L_{min}) is also lower in the semi-classical case compared to the quantum confinement case. This behavior is explained by comparing the Lateral Electric field (along the channel length) with the Electric Field along the thickness of the SOI fin for $T_{fin}=2$ nm and $T_{fin}=7$ nm over a wide range of gate and drain voltages. This analysis suggests that quantum confinement adversely affects the short channel effects and leads to an increase in the L_{min} compared to the semi-classical case. These results for L_{min} clearly illustrate the importance of the need to include the quantum confinement effects while evaluating the electrostatics performance and scalability of symmetric DG SOI FINFETs.

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1. Introduction

The Double-Gate (DG) Silicon-on-Insulator (SOI) FINFETs, schematically shown in Fig. 1, have been proposed as a viable option to extend CMOS scaling to and beyond the 65 nm technology node due to their ability to overcome inherent limitations of bulk silicon devices and provide improvement in device characteristics such as mobility, transconductance, integration density, reduced parasitic capacitance and short-channel effects (SCEs) [1]. As suggested by Chen et al. [2] for DG SOI MOSFETs/FINFETs and shown in Eq. (1) it is apparent that in order to scale down the gate length (L_g) to 25 nm and below, without significant SCEs, the SOI film thickness (t_{si})/Fin thickness (T_{fin}) must be very thin (Ultra-Thin-Body for planar DG SOI MOSFETs with $t_{si} \leq 10$nm and very thin fins for FINFETs with $T_{fin} \leq 10$nm) with a very high front/back oxide capacitance ($\frac{\epsilon_{ox}}{t_{ox}}$). This high oxide capacitance is achieved either through a very thin top and bottom gate oxide or through the use of a High-K gate dielectric.

$$\frac{T_{fin}}{2} + \left(\frac{\epsilon_{Si}}{\epsilon_{ox}}\right) t_{ox} \ll \frac{L_g}{2} \tag{1}$$

In Eq. (1), ϵ_{Si} and ϵ_{ox} are the permittivities of silicon and the gate-oxide (SiO_2), respectively. In Ultra-Thin (UT) Double-Gate SOI (DGSOI) devices which are fully depleted, reasonably good electrostatic control over the channel is possible provided the condition shown in Eq. (1) is satisfied. Eq. (1) is valid for SOI FINFET structures with extremely tall fins such that FINFET structure is effectively a DGSOI FINFET with the side gates depleting the Fin thickness. In our present work, we neglect the effects of tunneling and use a 1 nm thick SiO_2 side gate oxide, which in terms of capacitance is equivalent to a thicker High-K gate dielectric.

In the context of DG SOI MOSFETs, a number of past works [5–7] have suggested that due to very strong quantum confinement and poorer carrier transport properties, the minimum acceptable SOI film thickness could be about 5 nm. In UT DGSOI FINFETs, quantum confinement effects become significant for $T_{fin} \leq 10$nm, and turn out to be very dominant for $T_{fin} \leq 4.7$nm (excitonic Bohr radius of silicon). The impact of quantum confinement and device temperature variations on the electrostatics of long channel symmetric Double-Gate SOI MOSFETs/FINFETs was studied in our previous work [3,4]. In the long channel case, as the

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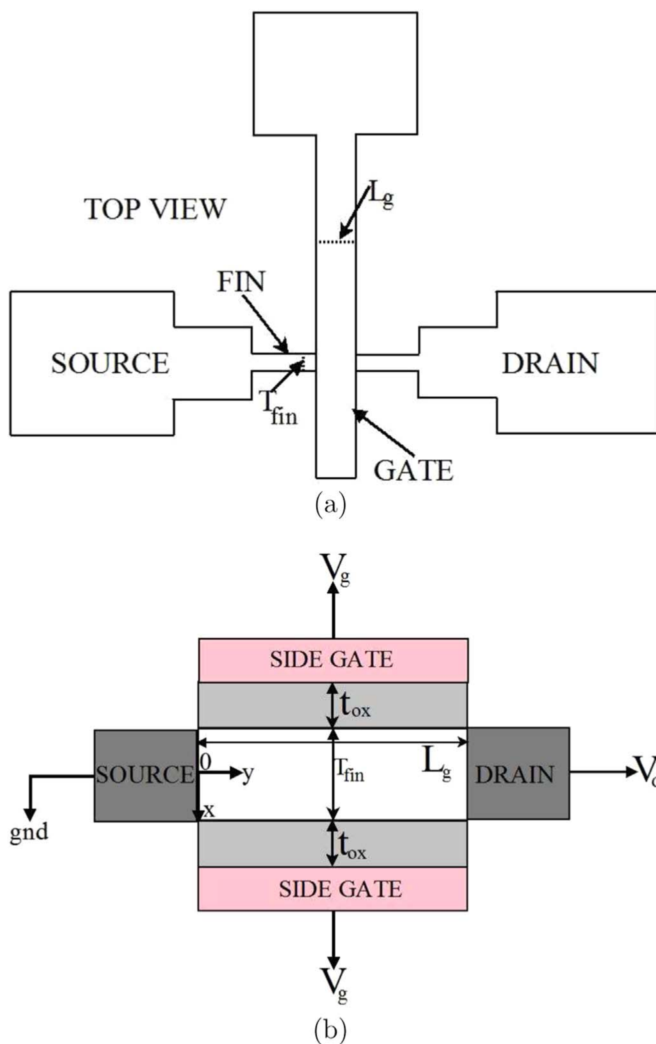

Fig. 1. (a) Top view of a FINFET. (b) Schematic diagram of a DG FINFET where x represents the direction along the direction of the silicon fin thickness and y represents the direction along the length of the channel. $x=0$ represents mid-point of the silicon fin i.e. silicon film extends from $x=-T_{fin}/2$ to $T_{fin}/2$.

effect of the drain voltage on the potential barrier between the source and channel was negligible, 1-D analysis was sufficient to analyze the electrostatics of such devices. It was noted that for a given fin thickness, the difference between the semi-classical and quantum confinement cases was primarily the higher threshold voltage due to the increase in band-gap (E_g) because of size quantization effects. However, these past reported works did not account for the impact of quantum confinement on the scalability of DG SOI MOSFETs/FINFETs, including the consideration of short channel effects. A detailed analysis of the impact of quantum confinement effect on the short channel effects in the Double-Gate SOI MOSFETS/FINFETs is extremely critical in determining the scalability of Double-Gate SOI MOSFETs/FINFETs.

In the past, 2-D Quantum-Mechanical (QM) simulations were conducted in conventional Silicon bulk MOSFETs [8] including short-channel effects in the channel electrostatics and it has been shown that compared to the semi-classical case, in the QM case, the sub-threshold slope, threshold voltage (V_{th}) and drain induced barrier lowering (DIBL) are higher. Similar studies have also been conducted for Ultra-Thin (UT) SOI MOSFETs with thick buried insulators [9] showing that QM effects suppress the buried insulator induced barrier lowering (BIIBL) effects thus adversely affecting the sub-threshold slope, leading to an increase in the threshold voltage roll-off due to the charge sharing effect, compared to the semi-classical case. However, for DG SOI MOSFETs, Chiang et al. [10] reported that the DIBL when considering QM effects would be lower due to opposing impacts of QM effects and SCEs on the threshold voltage, which was somewhat at odds with the findings by Omura et al. [9].

The most recent 14 nm FinFETs by Intel have a minimum gate length of 20 nm and fin thicknesses (T_{fin}) of 8 nm. As pointed out in a recent study [11], some of the important design criteria to enable FinFET design for future technology nodes (smaller channel lengths) without undermining the CMOS performance are the following:

- use an SOI structure (e.g local SOI in bulk Si);
- use an undoped Ultra-Thin-Body (UTB)/channel with t_{si} (T_{fin}) >4 nm;
- use Double-Gate (DG) as opposed to Triple-Gate (TG) architecture.

Hence, a more comprehensive 2-D analysis of the electrostatics of the DG SOI FINFET is required so as to account for the combined influence of T_{fin}, L_g and V_d (drain voltage) on the threshold voltage and the sub-threshold slope. This 2-D analysis, inclusive of the impact of quantum confinement effects on the electrostatics of DG SOI FINFETs, is also extremely essential in accurately determining the scalability of DG SOI FINFETs. This accurate 2-D analysis of the channel electrostatics of DG FINFETs is essential in terms of eventual 3-D analysis of the electrostatics of TG FINFETs. While the fin height (H_{fin}) is certainly an important dimension to consider, in the analysis of the electrostatics, it is also important to point out that since the fin height (H_{fin}) is generally much larger than (T_{fin}), the electrostatics of FINFETs is therefore more strongly dependent on the fin thickness (T_{fin}) and the channel length (L_g). Thus, in that sense, the analysis we have presented in the paper is extremely relevant not just in terms of determining the scalability of the DG SOI FINFETs but also eventually for TG FINFETs.

In this paper we present the results of a study obtained by analyzing the combined effects of fin thickness and the channel length reduction on the threshold voltage, sub-threshold slope and the drain induced barrier lowering. This paper also deals with another key issue of determining the ultimate scalability of the DG FINFETs when the quantum confinement begins to affect the gate/drain control of the Channel Charges [12]. In order to clearly distinguish the impact of quantum confinement on the electrostatics of Double-Gate (DG) SOI FINFETs, we consider two scenarios: (a) $T_{fin} < a_B$ (where a_B is the excitonic bohr radius of silicon equal to 4.7 nm) i.e $T_{fin} = 2$ nm (Strong Quantum Confinement regime). (b) $T_{fin} > a_B$ i.e $T_{fin} = 7$ nm (Weak Quantum Confinement regime). In order to obtain further insight into the impact of quantum confinement on the electrostatics of symmetric DGSOI FINFETs having shorter channel lengths, we also analyze and compare the electrostatics of these FINFETs for the two cases where quantum confinement effects are (a) Considered (Quantum Confinement case) and (b) ignored (Semi-Classical case). Based on this analysis, we determine the channel length, L_{min}, which corresponds to the transition between long channel and short channel behavior for the semi-classical and quantum confined cases. This also provides further insight into the relative impact of short-channel effects (SCEs) on the electrostatics of DG SOI FINFETs for the semi-classical and quantum confined cases. The analysis of the electrostatics presented in this paper including the investigation on the DG SOI FINFET scalability is confined to side gate voltages up to the threshold voltage, therefore, neglecting the direct tunnelling current may not induce significant inaccuracy in the results [13]. However, we do recognize that direct tunnelling current is significant for a 1 nm thin SiO_2 layer and intend to more

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