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New pulse amplitude modulation for fine tuning of memristor synapses ☆

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A B S T R A C T

Nanoscale memristors can be used as synapses in brain-mimicking neuromorphic systems. Here, the fine tuning of memristor conductance is important in controlling the synapse weights precisely, because the coarse tuning of memristor synapses can cause a significant error in neuromorphic processing. In this paper, we propose a new Pulse Amplitude Modulation (PAM) method for the fine tuning of memristor conductance. The new PAM scheme is verified by the experimental measurement of real memristors, where the new PAM could reduce the pulse-to-pulse fluctuation in conductance change per pulse by 84.8%, compared to the previous linear PAM. For comparing the linear and new PAM schemes, they are tested in programming memristor synapses in the memristor-based Cellular Neural Networks (CNN). The simulation result confirms that the new-PAM-programmed CNN shows better quality of edge detection than the linear-PAM-programmed CNN.

1. Introduction

In 2008, memristors were experimentally demonstrated by HP researchers [1]. Since then, many researchers have started to think that memristors may be useful in mimicking the synaptic function of neuronal systems because they can be made of nano-scale devices and consume lower power, compared to the CMOS circuits [2,3]. The conceptual diagram of memristor-based synapse is shown in Fig. 1(a), in which memristors act as synapses connecting the pre-neurons with the post-neurons. This is due to the fact that the memristance change by the history of charge or current flux seems very similar to the synaptic weight's change of biological neural systems [4,5]. Moreover, memristors are implementable in nano-scale and can be stacked layer by layer for possible 3-dimensional array architecture [6–8]. Due to all these advantages of memristors, the memristor-based synaptic circuit can be thought as a viable technique to implement the neuromorphic systems in future. One more thing to note here is that the fine tuning of memristor's

conductance is important in controlling synaptic weight precisely in neuromorphic circuits [9–15]. The coarse tuning of synapses can cause a significant error in neuromorphic signal processing as will be discussed more in detail in Section 3.

To use memristors as synapses in neuromorphic circuits, we need to program memristors until their conductance values reach the target synaptic weights, as the synaptic weights in neuronal systems are adjusted according to the external stimulation [9,14,15]. For programming memristors until the target weights, a pulse train should be applied to memristors to change their conductance values gradually until they reach the target ones [14–16]. Fig. 1(b) shows the measured memristor's conductance in the left y-axis and the conductance change per pulse in the right y-axis, when the pulse train with the amplitude of 2 V and duration of 100 μs is applied. Here, it should be noted that the amplitude of voltage pulses is unmodulated regardless of the number of pulses. In Fig. 1(b), the memristor's conductance is increased logarithmically and then saturated with increasing the number of pulses. Such the logarithmic saturation of memristor's conductance is commonly found in many memristive devices [14–16]. The logarithmic saturation of memristor's conductance results in the coarse tuning of memristor synapses which can degrade the performance of the memristor-based neuromorphic systems, as stated earlier [12–15].

Due to this logarithmic saturation, the memristor's conductance change per pulse seems decaying with increasing the number of programming pulses, as shown in Fig. 1(b). When the programming pulse train is started, the memristor's conductance

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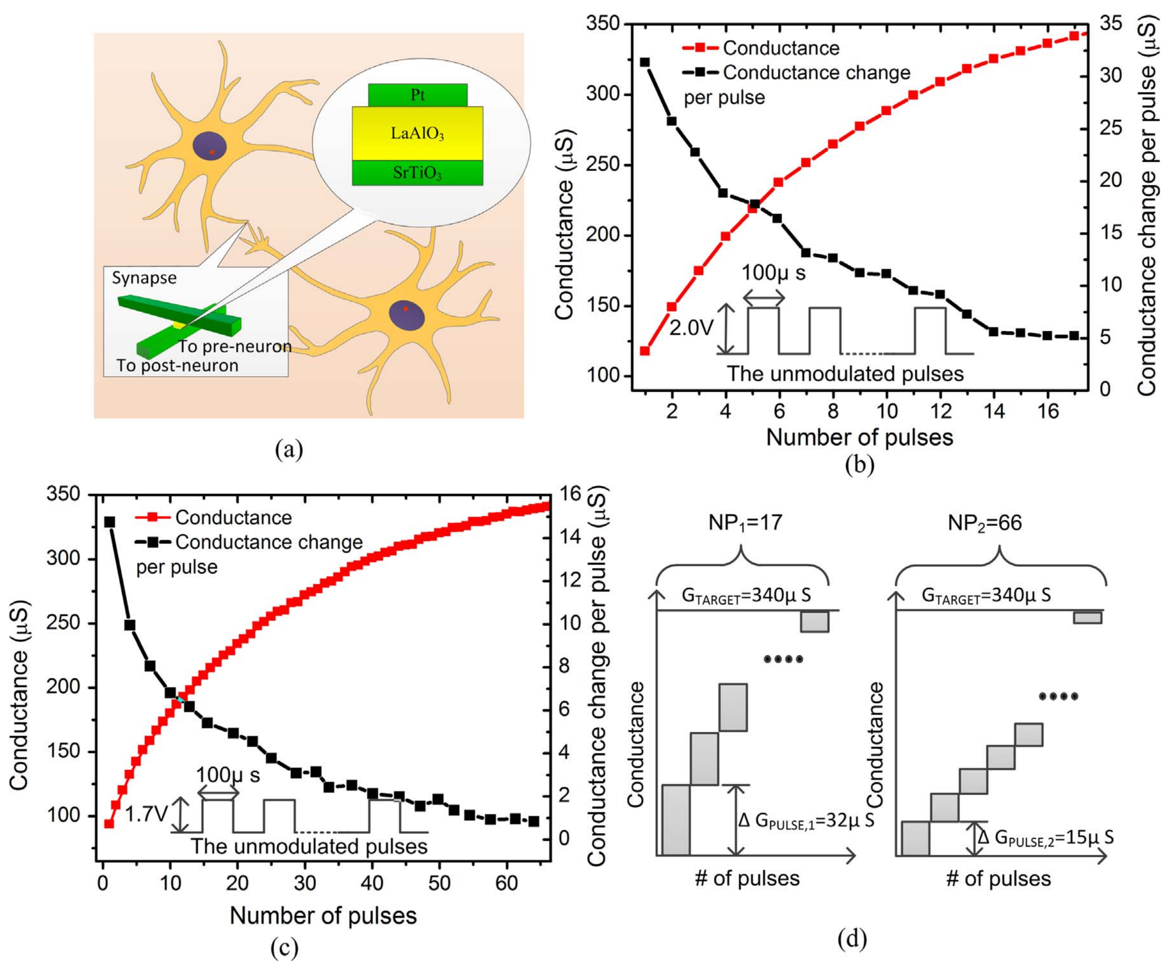

Fig. 1. (a) The schematic illustration of the concept of using memristors as synapses [4,5]. The insets show the schematics of the two-terminal device geometry and the layered structure of the memristor. (b) The measured memristor's conductance and the conductance change per pulse with increasing the number of pulses. The inset shows the unmodulated programming pulses with the voltage amplitude of 2 V and the pulse width of 100 μs. (c) The measured memristor's conductance and the conductance change per pulse with increasing the number of pulses. The inset shows the unmodulated programming pulses with the voltage amplitude of 1.7 V and the pulse width of 100 μs. (d) The relationship of the conductance change per pulse and the number of pulses. Here the applied pulse amplitudes are 2 V and 1.7 V. Both the pulse amplitudes of 2 V and 1.7 V show the logarithmic saturation of memristor's conductance according to the pulse train. The 2-V pulse train has $\Delta G_{PULSE,1}=32$ μS and needs 17 pulses to reach $G_{TARGET}=340$ μS. The 1.7-V pulse train has $\Delta G_{PULSE,2}=15$ μS and needs 66 pulses to reach $G_{TARGET}=340$ μS. In both cases, the conductance changes per pulse of the 2-V and 1.7-V trains are decreased with increasing the number of programming pulses. Here NP_1 and NP_2 are the number of pulses to reach G_{TARGET} for the 2-V and 1.7-V pulse train, respectively.

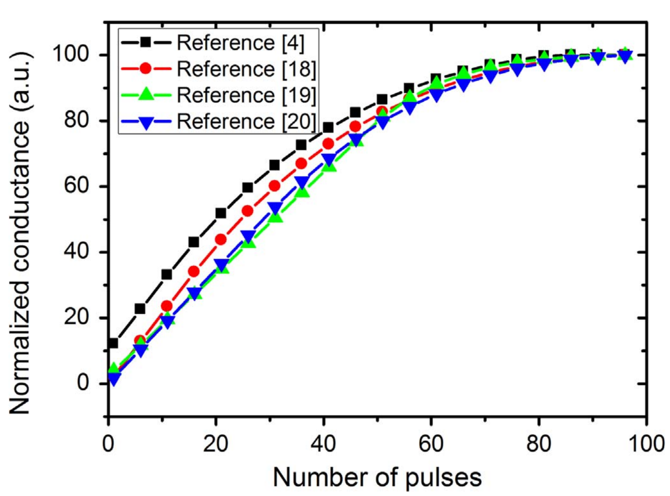

Fig. 2. The normalized memristor's conductance with increasing the number of programming pulses. The normalized conductance values in this figure are calculated from the memristor's behavioral model. We calculated the conductance values in this figure using the model parameters [17] which were obtained from the measured data of various memristors [4,18–20].

change per pulse is as large as 32 μs. But, the conductance change per pulse becomes smaller and finally saturated with increasing the number of programming pulses, in Fig. 1(b). For example, when the number of pulses is 17, the conductance change per pulse becomes as small as 5.2 μs, as shown in Fig. 1(b).

Fig. 1(c) also shows memristor's conductance and conductance change per pulse in double-y plot, for the pulse amplitude of 1.7 V. In Fig. 1(c), the conductance change per pulse is smaller than that one in Fig. 1(b), because the amplitude is lowered from 2 V to 1.7 V.

The relationship of the conductance change per pulse and the number of programming pulses is depicted in Fig. 1(d). Here, the applied pulse amplitudes are 2 V and 1.7 V. Both the pulse amplitudes of 2 V and 1.7 V show the logarithmic saturation of memristor's conductance according to the pulse train. $\Delta G_{PULSE,1}$ is the conductance change per pulse in Fig. 1(b) with 2-V amplitude. When the programming pulse train starts, $\Delta G_{PULSE,1}$ is large. As the number of programming pulses is increased, $\Delta G_{PULSE,1}$ becomes smaller, as illustrated in Fig. 1(d). Similarly, $\Delta G_{PULSE,2}$ is the conductance change per pulse in Fig. 1(c) with 1.7-V amplitude. To reach the target conductance of 340 μs, $\Delta G_{PULSE,1}$ and $\Delta G_{PULSE,2}$ need 17 and 66 pulses, respectively, as shown in Fig. 1(d).

The logarithmic saturation in memristor's conductance can be