Microelectronics Journal 49 (2016) 19–28

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Ka-band frequency synthesizer involving a varactorless *LC*-type voltage-controlled oscillator and phase rotation

Jun-Hong Weng *, Shen Cheng, Chih-Kai Chiu, Chih-Hsiang Chang

Department of Electrical Engineering, Tunghai University, 1727, Sec. 4, Taiwan Boulevard, Taichung 40704, Taiwan

ARTICLE INFO

Article history:
Received 28 April 2015
Received in revised form
1 September 2015
Accepted 10 December 2015
Available online 14 January 2016

Keywords:
Frequency doubler
Frequency synthesizer
Quality factor
Tuned transducer
Varactorless
Voltage controlled oscillator (VCO)

ABSTRACT

This paper discusses the design and fabrication of a high-frequency wide-range frequency synthesizer based on a phase locked loop (PLL), varactorless *LC*-type voltage-controlled oscillator, and push–push frequency doubler. In addition, a high-speed programmable divider using multiphase selection is employed for channel switching. The proposed circuits were fabricated in a standard 90-nm CMOS process with a chip area of 0.8 mm × 1.1 mm. The PLL dissipated 60 mW when the supply was 1.2 V. The measured phase noise of the frequency synthesizer at a frequency of 17.64 GHz and offset of 1 MHz was −97 dBc/Hz.

1. Introduction

Most wireless transceivers include a frequency synthesizer for generating a local oscillator (LO) signal from a low-frequency crystal oscillator. The receiver is based on a dual-conversion architecture, which reduces the system complexity substantially, and a single LO can be used to simplify frequency planning and building block design [1]. Fig. 1 depicts a receiver architecture with two down-conversion stages; two LO frequencies (f_1 and $f_2=f_1/2$) are used to generate quadrature phases.

In Fig. 1(a), the quadrature LO is generated by a divide-by-two circuit, avoiding the power-hungry polyphase filter [2]. LO-related problems are so severe at millimeter-wave frequencies that the choice of the receive (RX) and transmit (TX) topologies becomes closely intertwined with the LO design. The frequency synthesizer is of the phase locked loop (PLL) type, which is one of the most power-consuming blocks in the transceiver. High-frequency components for PLL design are critical in the trade-off between high frequency, low power, and wide-range operations.

To ameliorate the aforementioned difficulties, an alternative approach, depicted in Fig. 1(b), uses a simple and low-cost architecture employing a voltage-controlled oscillator (VCO) as the second LO and a frequency doubler (FD) as the first LO. This alternative relies on a frequency multiplier circuit driven by the VCO running at a lower frequency [3]. As a result, a half-rate VCO combined with a frequency doubler can provide a more reasonable tuning range than can a full-rate VCO with a divide-by-2 circuit. In the frequency-multiplying circuits, the most effective solution exploits the nonlinearity of active devices to generate harmonics of the input signal.

To maximize both the tuning range and operating frequency of a VCO, appropriately designing the capacitances in the tank is crucial. The capacitances can be formed from an effective parasitic capacitor and a varactor, and their values can be considered as the sum of a voltage-controlled variable capacitance and a nonvariable capacitance. The main contribution to the nonvariable capacitance derives from the parasitic effects of the inductor, varactor, and transistors; this capacitance limits the tuning range of the VCO, even reducing the operating frequency, because it cannot be varied by the controlled voltage. The VCO has the disadvantage of a trade-off between the dynamic range and operating frequency. However, this disadvantage can be overcome by using standard CMOS processes. Thus, a varactorless *LC*-type VCO featuring a tuned-transducer topology is proposed in this paper [4,5].

Because most wireless systems operate in a narrow frequency band, the frequency doubler of the VCO, which is narrowband, can be used to achieve a trade-off between the bandwidth and the power and maximal operating frequency. Consequently, a higher frequency and lower power operation can be achieved.

A high-frequency programmable divider capable of high-resolution frequency switching is a critical component in PLL applications in

* Corresponding author. Tel.: +886 4 23590121x33910.
E-mail address: jhw@thu.edu.tw (J.-H. Weng).

http://dx.doi.org/10.1016/j.mejo.2015.12.009
0026-2692/

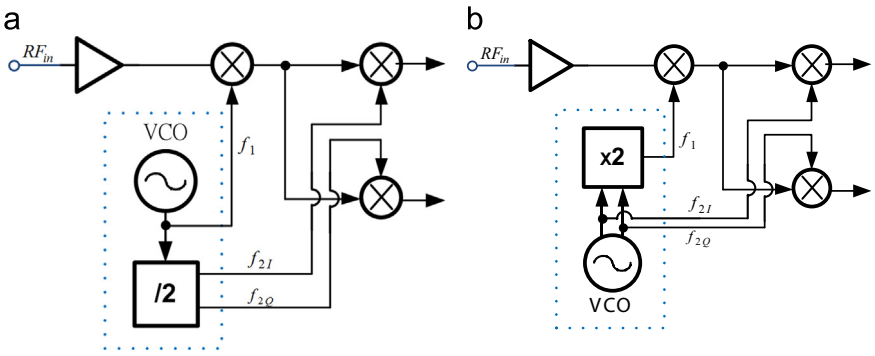

Fig. 1. Receiver architecture and an example of frequency planning: (a) LO signal generation using a VCO and a divide-by-2 divider and (b) LO signal generation using a VCO and a frequency doubler.

wireless communication. The divide-by-two scheme involving a toggle flip-flop or injection division is generally employed in high-frequency prescalers because of its simple architecture. However, such prescalers have a fixed division ratio and cannot provide dual-mode functionality when used as swallow dividers. Consequently, the overall resolution of a high-speed frequency synthesizer is reduced.

In this study, a frequency synthesizer comprising a varactorless VCO, frequency doubler, and high-frequency programmable divider was demonstrated; the frequency synthesizer was fabricated using a 90-nm CMOS process for high-frequency operation. The circuits involved exhibited several improved features compared with existing circuits. First, the varactorless VCO was developed using a combination of mutual-negative-resistance [6] and negative-transconductance techniques to extend the operating frequency range [7]. Second, the frequency doubler behind the VCO had a push-push structure with a notch filter to achieve high fundamental rejection [8]. In addition, to maintain the inherent channel resolution for the PLL, a high-frequency multimodulus divider and a phase rotation technique were used to enable the phase selector to operate the multichannel PLL. The remainder of this paper is organized as follows. The basic concept of the frequency synthesizer system architecture is presented in Section 2. Section 3 describes implementing the building blocks. Experimental results are presented in Section 4, and Section 5 concludes the paper.

2. Basic system architecture

2.1. Architecture

Fig. 2 shows the proposed high-frequency PLL-based frequency synthesizer, which consists of a phase frequency detector (PFD), charge pump (CP), low-pass filter, varactorless *LC*-VCO, frequency doubler, and multimodulus divider with a three-bit accumulator for multimodulus control.

Following the voltage-controlled oscillation, the divide-by-8 prescaler with eight-phase outputs acted as a fractionally programmable divider, enabling multiphase switching in the digiphase synthesizer and thereby reducing periodic tones through phase error cancellation before the signal was provided to the PFD. The division ratio, dependent on the logic value at the mode control, ranged from 120 to 127. To achieve a high-frequency and wide-range design, a frequency doubler was employed at the output stage, enabling VCO operation at a frequency of only half the output frequency of the synthesizer. Thus, the output synthesized frequency is expressed as $f_{vco} = N \cdot f_{ref}$ (i.e., $f_{out} = 2 \cdot N \cdot f_{ref}$), where N is an integer from 120 to 127.

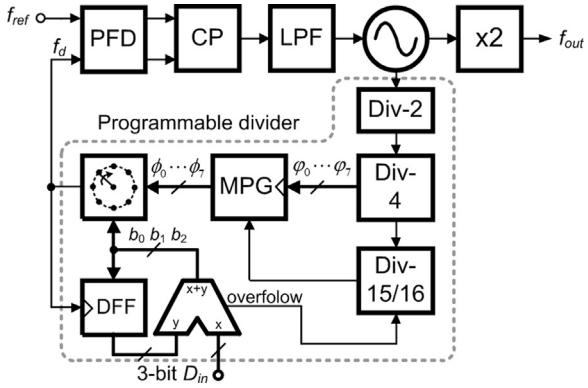

Fig. 2. Block diagram of the frequency synthesizer.

2.2. Concept of multimodulus divider

The multimodulus divider comprised a high-speed divide-by-8 prescaler, phase rotator, logic controller, and integral divider with a dual-mode divide ratio of 15 and 16. In the prescaler, the high-speed divide-by-4 divider enabled conveniently generating multiple phases with a difference of $T_P/8$, where $T_P = 8T_{VCO}$. The dual-modulus divider was used to divide the prescaler frequency by 15/16; phase compensation from the phase generator and rotator performed fractionally. The divide fractional ratio can be represented as $(15+k/8)$, where k is a 3-bit value. An output waveform with a multichannel period was generated. For example, for a desired fractional value of 1/8, the phase rotator multiplexed the phase-shift waveforms in the cyclic sequence $\phi_0 \rightarrow \phi_1 \rightarrow \cdots \rightarrow \phi_7 \rightarrow \phi_0 \rightarrow \cdots$, and the output period of the fractional divider was $T_d = (15+1/8) \cdot T_P$ (Fig. 3).

The division ratio should periodically switch from 15 to 16 when the output waveforms from ϕ_0 to ϕ_7 are multiplexed. For arbitrary k, the output period T_d can be calculated as

$$T_d = \left(15+\frac{k}{8}\right)T_P = (120+k)T_{VCO} \quad (1)$$

Thus, the divide ratio of the multimodulus divider can be demonstrated by (1).

3. Main circuit implementation

3.1. Frequency divider

The PLL contained a divide-by-128 frequency divider comprising a two-stage high-speed current-mode logic (CML)-like divide-by-two divider and a five-stage digital static flip-flop-based divide-by-two divider. The CML-like divider [9] contained a master–slave D flip-flop