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TCAD RF performance investigation of Transparent Gate Recessed Channel MOSFET

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ABSTRACT

In this paper, analog/RF performance and small signal behavior of Transparent Gate Recessed Channel (TGRC) MOSFET has been investigated in terms of transconductance, DIBL, channel resistance parasitic capacitances, cut-off frequency and maximum oscillator frequency. Results so obtained are compared with Conventional Recessed Channel (CRC) MOSFET at THz frequency range, using ATLAS-3D device simulator. Furthermore, the impact of technology parameter variations in terms of gate length (L_g) has also been evaluated. Result shows that there is 42% enhancement in cut-off frequency, 132% increment in maximum oscillator frequency and significant improvement in parasitic capacitances for TGRC-MOSFET due to reduced short channel effects (SCEs) and enhanced on-current driving capabilities thus, reflecting its significance in high-frequency THz range applications.
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1. Introduction

In the era of sub-100 nm dimensions, continuing scaling of conventional MOSFET is done to develop opportunities for further high speed and low power applications. Highly scaled MOSFETs achieved cut-off frequencies in several THz range making CMOS technology appropriate for RF application and wireless communications [1–4]. In the conventional MOSFET, as the channel length diminishes, the gate control over the channel is reduced due to increased source/drain capacitances [5]. However, with scaling down of the device dimensions, the so-called SCEs arises such as mobility degradation, hot carrier effects, drain induced barrier lowering, parasitic capacitances etc, making the scaled devices inapt for high-frequency wireless applications [6]. To overcome such effects, numerous device engineering schemes such as gate engineering, channel engineering etc. and novel device structures such as SOI MOSFET [7], Dual Gate MOSFET [8], Recessed Channel (RC) MOSFET [9], GAA MOSFET [10], Silicon Nanowire MOSFET [11] etc. have been reported in the literature.

SCEs are mainly caused by drain barrier width extending into the source region, resulting in barrier lowering. Thus, in terms of both functionality and cost, grooved gate MOSFET is the most promising one to avoid this potential extension [12]. In RC MOSFET, two potential barriers are formed at the corners due to the high density of electric field lines at the corners, which leads to SCE immunity. Moreover, carriers in the channel now require more energy to surmount these hurdles, which bounds its electron transport efficiency and hence, on-current capabilities of the device [13]. To overcome this drawback, we incorporate the concept of gate transparency on RC MOSFET.

In TGRC-MOSFET, the metal (Al) gate is replaced with a transparent conducting oxide [14,15] called indium tin oxide (ITO). ITO is a solid solution of indium oxide (In_2O_3) and tin oxide (SnO_2). It is transparent and colorless in thin layers. ITO is one of the most widely used transparent conducting oxides because of its two chief properties: its electrical conductivity and optical transparency as well as the ease with which it can be deposited as a thin film [16–18]. Moreover, due to the increased demand for high-speed electronics products, the accurate modeling of the MOSFETs at high frequencies (HF) is necessary to represent the behavior of device in microwave circuits and systems [19]. Transparent conducting oxide (TCO) semiconductor is essential to use in optoelectronic devices such as flat panel display. ITO is one of the TCO semiconductors which are mostly used in optoelectronic device applications. ITO is not normally available in the market because of cost and shortage of indium, the principle material of ITO [20].

In this work, the analog performance of TGRC-MOSFET [21,22] has been observed in terms of transconductance (g_m), drain current (I_D), conduction band and valence band, which reflects that TGRC-MOSFET is suitable for AC applications. Further, the present work stresses on

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the TCAD assessment of TGRC-MOSFET for high-performance RF applications in terms of figure of merits such as cut-off frequency, maximum oscillator frequency and parasitic capacitances. The most suitable method to observe the small signal behavior of MOSFET at high frequencies involves *S*-parameter measurements. *S*-parameters are commonly employed for those networks that are operating at RF and microwave frequencies, where energy analysis and signal power are more easily computed as compared to voltages and currents, since, at high frequencies it is very difficult to estimate the current and voltages. Short and open circuits (used by definitions of most *n*-port parameters) are hard to realize at high frequencies. As a result, microwave engineers work with so-called *S* parameters, which utilize waves and matched terminations. This approach also minimizes the reflection problems [23].Thereafter, the impact of parameter variation in terms of gate length is observed with sufficient enhancement in terms of cut-off frequency, maximum oscillator frequency, and parasitic capacitances in TGRC-MOSFET.

2. Device structure and its parameters

A schematic cross-sectional view of simulated device i.e. TGRC-MOSFET is shown in Fig. 1, which consists of the gate made up of transparent conducting material indium tin oxide as shown in Fig. 1(a). The total gate length is 30 nm and thickness of oxide is 2.0 nm. In this case, substrate doping is p-type with a concentration of 1×10^{17} cm^{-3}; source and drain are n-type with uniform doping profiles as 1×10^{19} cm^{-3}. Table 1 shows the default parameters of the device structure.

Here, RF performance, which is determined by the figure of merits such as cut-off frequency, maximum oscillator frequency, parasitic capacitances, maximum available power gain and maximum stable power gain, are investigated by extensive device simulations for 30 nm gate length-CRC-MOSFET and TGRC-MOSFET. Further, the RF performance of CRC-MOSFET and TGRC-MOSFET has been studied under the bias condition (V_{GS}=0.7 V, V_{DS}=0.5 V and frequency range from 0 to 1.8 THz) and a comparative analysis has been performed.

3. Simulation methodology

All simulations have been performed using ATLAS and DEVEDIT 3D device simulator [24]. For the simulations, authors adopted physical models accounting for the electric field-dependent and concentration-dependent carrier mobilities, Shockley–Read–Hall recombination/generation with doping dependent carrier lifetime, inversion layer Lombardi CVT mobility model, wherein concentration-dependent mobility, high field saturation model are all included [24]. We have adopted the hydrodynamic energy transport model instead of drift-diffusion method which incorporates all non-local effects into account.

4. Calibration

Calibration of model parameters used in simulation has been performed according to the published results obtained by Chaujar et al. [25] using above models and the obtained calibrated results are shown in Fig. 2.

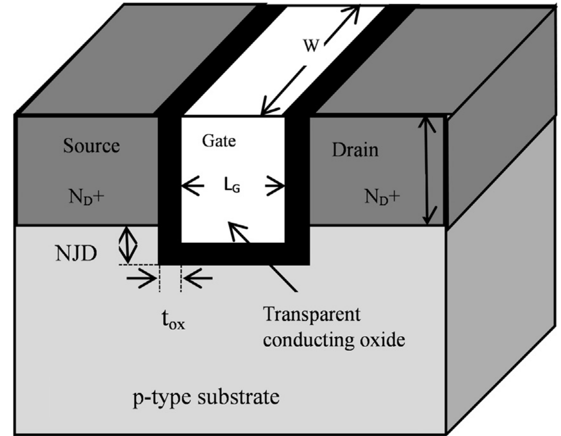

Fig. 1. Schematic structure of Transparent Gate Recessed Channel MOSFET.

Table 1
Design parameters of CRC-MOSFET and TGRC-MOSFET device designs.

Parameters	Unit
Channel length (L_G)	30 nm
Device width	200 nm
Groove depth	38 nm
Source/drain junction depth	30 nm
Negative junction depth (NJD)	10 nm
Substrate doping (N_A)	1×10^{16} cm^{-3}
Source/drain doping ($N_D{}^+$)	1×10^{19} cm^{-3}
Physical oxide thickness (t_{ox})	2 nm
Permittivity of SiO_2	ε_{ox}=3.9
Gate to source voltage (V_{GS})	0.7 V
Drain to source voltage (V_{DS})	0.5 V
Work function for TGRC-MOSFET (Φ_{ITO})	4.7 eV
Work function for CRC-MOSFET (Φ_M)	4.2 eV

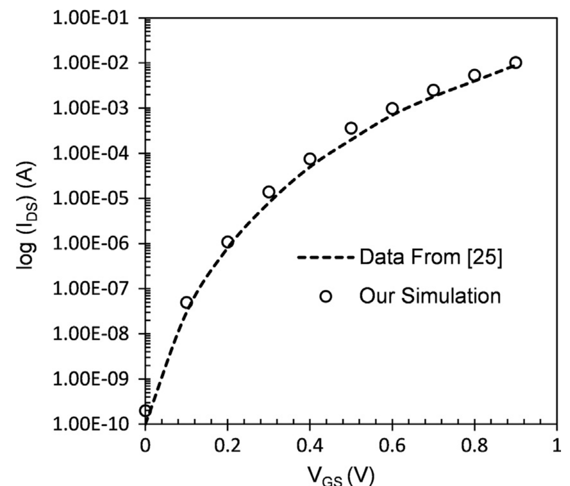

Fig. 2. Calibration with the published result, $I_{DS}-V_{GS}$ characteristics of 40 nm gate length TGRC-MOSFET.

5. Results and discussions

5.1. Analog performance metrics analysis

5.1.1. Transfer characteristics and Transconductance

Fig. 3(a) and (b) shows the drain current and transconductance profile respectively, for CRC-MOSFET and TGRC-MOSFET. Transparent conducting oxide gate is used instead of a metal gate in TGRC-MOSFET, which enhances the drain current and hence the transconductance as shown in Figs. 3 and 4 respectively, due to improved

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