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A low power low noise amplifier employing negative feedback and current reuse techniques

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ABSTRACT

This paper presents a low power wideband differential Low Noise Amplifier (LNA) suited for multimode receivers and Wireless Sensor Networks (WSN) in a 0.18 µm CMOS technology. By using negative feedback, the stringent trade-off between the input matching and the transconductance (g_m) is broken and the required transconductance of input transistor in Common-Gate (CG) LNA is decreased. As a result of this and also using the current reuse implementation scheme, power consumption (P_{DC}) is significantly reduced. The circuit provides high gain and decreased Noise Figure (NF) in spite of low P_{DC}. The LNA structure is fully inductorless, and the core circuit consumes only 1.3 mW from a 1.8-V supply occupying an area of 0.032 mm^2. A maximum voltage gain of 20.1 dB is provided with 3 dB bandwidth up to 3.3 GHz. The input matching is better than −16 dB from 20 MHz to 3.3 GHz. The minimum NF is 3.2 dB with third order Input Intercept Point (IIP$_3$) of −2.4 dBm.

1. Introduction

Wideband Low Noise Amplifiers are used in multi-standard applications which support several standards (e.g. cellular communications at 900 and 1800 MHz, global positioning system at 1.2 and 1.5 GHz, Wi-Fi at 2.4 GHz, and etc.) simultaneously [1–5]. The conventional solution for multiband receivers is to employ several LC-tuned LNAs in parallel [6,7]. This approach consumes very large die area. Thus, complexity is added to receiver design. In contrast, wideband LNAs significantly reduce cost, area, and power.

Several methods have been presented to provide input matching for wideband amplifiers, such as the distributed amplifier [8], filter-type amplifier [9], and resistive shunt feedback amplifier [10]. These methods suffer from high power consumption, large chip area and relatively high NF. Although noise canceling technique is used in wideband LNAs to achieve lower NF [11–14], the respective topologies often require high power consumption. One of the wideband LNA topologies is the Common-Gate LNA. The CG-LNA is appealing compared to other topologies owing to wideband input impedance matching, furthermore, good linearity and stability is offered. Moreover, techniques such as dual negative feedback [1], multiple negative–positive feedback [2], noise canceling with current amplification [12], gain enhanced noise canceling [13], or noise canceling with the use of PMOS transistors and current reuse technique [14] are used to overcome the trade-off between input matching and NF in CG-LNA. However, the power consumption of CG-LNA is higher than common-source L-degenerated LNAs. This drawback is due to the input matching condition, which imposes a certain value of transconductance and consequently, relatively significant amount of power consumption [21].

In this paper a differential wideband CG LNA employing negative feedback is proposed. Utilizing this technique, the intense trade-off between input matching and power consumption has been eliminated. As a result, power consumption is lowered while the desired input matching is realized. Further, current reuse is utilized to more reduction in power consumption. Since the structure is inductorless and the power consumption is low, the LNA can be easily employed in Wireless Sensor Networks (WSN), such as ZigBee standard and multi-standard applications.

This paper is organized as follows. In Section 2 a review of design techniques for inductorless LNAs is given. The proposed technique is presented in Section 3. Section 4 includes post layout simulation results. Finally, Section 5 concludes the paper.

2. Review of design techniques

Among the various LNA topologies suited for wideband operation, shunt feedback (SFB) and common-gate topologies are the most widely used structures. The shunt feedback technique is

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applied through either impedance-based SFB amplifier (Fig. 1a) [15] or source-follower-based SFB amplifier (Fig. 1b) [3,4] and [16]. Major weak point of impedance based SFB amplifiers is the limited value of output impedance ($Z_F||R_L$). Thus, it demands larger g_m value and increased power consumption to achieve a high gain. Although, the use of gain enhanced noise canceling technique removes the trade-off between voltage gain and NF in impedance-based SFB amplifier [13], the power consumption is very high.

Source-follower-based SFB technique is proposed to decouple the output from input impedance. The Resistor R_f in the feedback path is used to enhance the linearity of the circuit [3,16]. óNonetheless, nonlinearity of source-follower transistor degrades linearity-gain trade-off. Moreover, this structure exhibits poor NF and linearity performance in case of using very low g_m values (i.e., few mS). Additionally, extra DC power (P_{DC}) is required to realize functional feedback. Current reuse technique [3] can slightly improve NF and power consumption of the structure. Also, the use of source follower based SFB amplifier in balun LNA scheme (single input, differential output structure) [4] cancels out noise and distortion of feedback transistor and can achieve better performance. However, it's power consumption is high.

In order to elevate the functionality of SFB amplifiers, the CG topology can be replaced. CG circuits excel in linearity, stability and lower power consumption compared to SFB. For the conventional differential CGLNA (Fig. 2a) input matching constraints compels g_{m1} to be equal to $1/(50\,\Omega)=20$ mS [2]. Assuming this condition, the noise factor is given by

$$F=1+\frac{\gamma}{\alpha}+\frac{\gamma}{\alpha}g_{m2}R_S+\frac{4R_S}{R_L} \tag{1}$$

where γ is the excess channel thermal noise coefficient, and α is the ratio between g_m and the zero-bias drain conductance g_{d0}. The second term in (1) denotes the noise contribution of tail transistor, which is often replaced by an off-chip inductor to achieve low noise figure. It can be observed that in the CG-LNA, stringent constraints on g_m result in relatively high power consumption and noise factor. Recently, several papers avoided the P_{DC}-g_m trade-off in CG amplifiers by applying active or passive g_m-boosting technique [17–21].

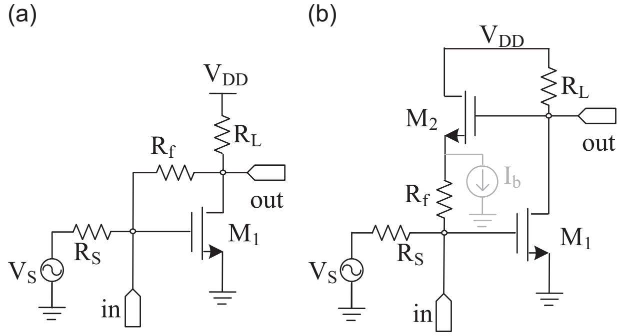

Fig. 1. Shunt Feedback LNA: (a) impedance-based SFB LNA, (b) source-follower-based SFB LNA.

G_m-boosting technique (Fig. 2b) enhances the effective transconductance by a factor of $(1+A)$, simultaneously reducing the NF and needed power consumption by the same factor compared with the CG-LNA, where A is the gain of boosting amplifier.

However, the noise and P_{DC} contribution of the auxiliary amplifier which is typically a CS amplifier [19] degrades these improvements. It is expected to have this problem eliminated by using an inductive transformer [20]; however, a large extra silicon area will be required.

Capacitive Cross Coupling (CCC) CG-LNA (Fig. 2.c) is a special case of g_m-boosting technique, in which a passive unit gain is used as boosting amplification [17,18]. In [5] and [21] the authors blend the active g_m-boosting and CCC techniques, to further reduction of P_{DC}.

Due to large swing in V_{GS}, the major disadvantage of g_m-boosting technique is degraded linearity of circuit. The IIP_3 of the gm-boosted LNA using IIP_3 and IIP_2 of both main and boosting amplifier can be expressed as [19,21]

$$\frac{1}{IIP_3{}^2}=\frac{(1+A)^2}{IIP_{3-CG}{}^2}+\frac{A}{(1+A)IIP_{3-BOOST}{}^2}+\frac{3}{2}\cdot\frac{A}{IIP_{2-CG}.IIP_{2-BOOST}} \tag{2}$$

If we Assume that $A\gg 1$ and both $IIP_{2\text{-}CG}$ and $IIP_{2\text{-}BOOST}$ are very high given the differential structure, the IIP_3 of the gm-boosted circuit is lower than the CG-LNA divided by a factor $(1+A)$. So, practically the g_m-boosting technique is only useful for the CCC CG-LNA [12]. However, in this case, g_m of the input transistors must be higher than $1/2R_S=10$ mS.

Table 2 summarizes the main properties of the LNA structures that have been discussed in this section. In the next section, we propose a technique in which CCC g_m-boosting is implemented while a negative feedback is added to lower the required g_m value for input matching, without any negative impact on linearity of circuit.

3. Proposed Common-Gate LNA (CG-LNA)

3.1. Concept of the proposed LNA

The main idea is utilizing a technique to eliminate the trade-off between input matching and power consumption by using the transconductance of the tail transistor. Fig. 3a represents the concept in realization of the proposed idea. In this conceptual

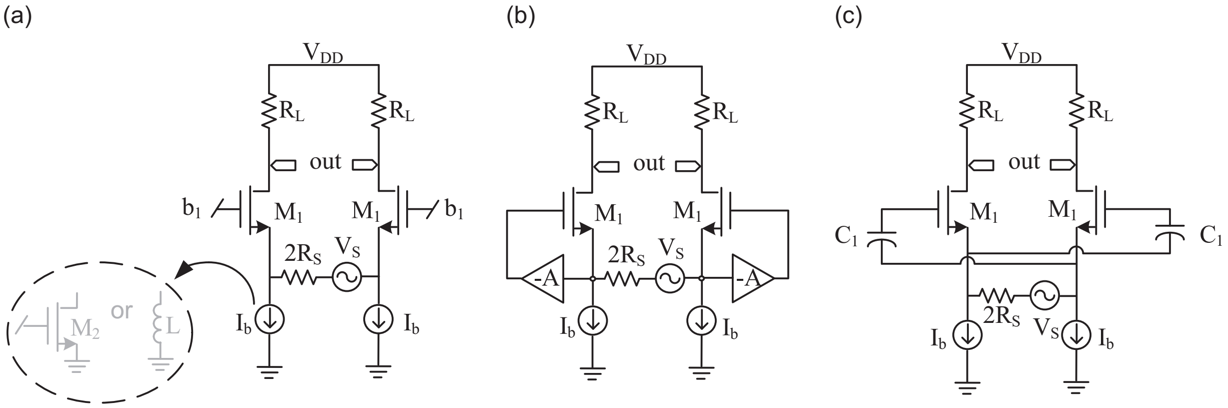

Fig. 2. Conventional Common Gate structures: (a) CG LNA, (b) Gm-boosted LNA, (c) Capacitively Cross Coupled LNA.