Microelectronics Reliability 50 (2010) 351–355

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

The frequency-dependent electrical characteristics of interfaces in the Sn/*p*-Si metal semiconductor structures

Ş. Karataş [a,*], A. Türüt [b]

[a] Department of Physics, Faculty of Sciences and Arts, University of Kahramanmaraş Sütçü İmam, 46100 Kahramanmaraş, Turkey
[b] Department of Physics, Faculty of Sciences and Arts, Atatürk University, 25240 Erzurum, Turkey

ARTICLE INFO

Article history:
Received 10 July 2009
Received in revised form 12 October 2009
Available online 9 February 2010

ABSTRACT

The purpose of this paper is to investigate frequency-dependent electrical characteristics of the interface states in Sn/*p*-Si metal semiconductor (MS) Schottky structures. To yield quantitative information about their frequency (f) and voltage (V) dependent characteristics, Sn/*p*-Si MS structures have been studied by using capacitance (C) and conductance (G/ω) measurements over a wide range of frequencies (50 kHz–1 MHz). The increase in capacitance at lower frequencies is seen as a signature of interface states, and the densities of which are evaluated to be of the order of $\cong 10^{10}$ cm^{-2} eV^{-1}. The presence of the interfaces states (N_{SS}) is also evidenced as a peak in the capacitance–frequency characteristics that increases in magnitude with decreasing frequencies. Furthermore, the voltage and frequency dependence of series resistance (R_S) were calculated from the C–V and G/ω–V measurements and plotted as functions of voltage and frequency. The effect of R_S on C and G/ω is found noticeable at high frequencies. The C–V–f and G/ω–V–f characteristics of studied structures show fairly large frequency dispersion especially at low frequencies due to N_{SS} in equilibrium with the semiconductor. The experimental values of interface state densities and series resistance from C–V–f and G/ω–V–f measurements were obtained in the ranges of 3.46×10^{10}–1.26×10^{9} cm^{-2} eV^{-1} and 71.1–57.3 Ω, respectively. Experimental results show that both the R_S and N_{SS} values should be taken into account in determining frequency-dependent electrical characteristics.

1. Introduction

Metal-semiconductor (MS) Schottky structures are an essential part of virtually all semiconductor electronic and optoelectronic devices [1–6]. Due to the technological importance of the metal-semiconductor structures which are of the most simple of the MS contact devices, a full understanding of the nature of their electrical characteristics is of greater interest [1–10]. In particularly, Si-contacts play one of the most important roles in Si-device or technologies represented by integrate circuit (IC), large-scale integration (LSI) and very-large-scale integration (VLSI). The role of the contacts is to interconnect individual devices (transistors, diodes and so on) in a Si chip and connect them as a whole to the outer circuit. These contacts are numerous in a chip and can easily total more than one million [6]. The performance and reliability of these structures are especially dependent on the formation of insulator layer between metal and semiconductor interface and series resistance of structures. Also, the changes in frequency and voltage have an important effect on determination of the MS structures [7,8]. Therefore, the frequency and voltage dependence electrical properties of MS structures are very important for different applications.

The interface states and series resistance values of metal-semiconductor structures are important parameters that affect their main electrical parameters [9–12]. The values of the capacitance and conductance depend on various parameters, such as density of surface states, series resistance, insulator layer thickness and barrier height formation between metal and semiconductor. Therefore, the capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristics of a metal semiconductor structure are extremely sensitive to interface state density at the MS interface [12–21]. When voltage is applied across the MS device, the combination of the interfacial insulator layer, depletion layer and the series resistance of the device will share applied voltage. Furthermore, some investigations [11,12,22] have reported an anomalous peak in forward C–V characteristics. The origin of such peaks has been ascribed to the interface states [12] and to the series resistance effect [22,23]. It has been shown that the interface states density strongly depends on frequency, and exponentially decreases with increasing frequencies. The C–V curves give peak in the depletion region due to the particular distribution of interface states between Sn/*p*-type Si interface and effect of series resistance, respectively. The position of peaks in the C–V curves is shifting towards reverse

* Corresponding author. Tel.: +90 344 219 1310; fax: +90 344 219 1042.
E-mail address: skaratas@ksu.edu.tr (Ş. Karataş).

0026-2714/$ - see front matter © 2009 Elsevier Ltd. All rights reserved.
doi:10.1016/j.microrel.2009.10.017

bias region with increasing frequency and almost disappears at high frequencies. This occurs because at lower frequencies the interface states can follow the ac signal and yield an excess capacitance, which depends on the frequency. However, the values of the capacitance at the high frequency region originate from only space charge capacitance, and at higher frequencies (as described above) interface states cannot follow the alternating current (ac) signal [1,2,14,15,22,23]. Thus, the series resistance (R_S) and interface states density values (N_{SS}) at metal-semiconductor structures play an important role in the determination of the main parameters of the structures. In general, the C–f and G/ω–f plots in the idealized case are frequency-independent [23,24]. Thus, characterization of MS Schottky structures can be electronically made by conductance technique [7]. Since the interface excess capacitance depends on the frequency, the capacitance peak in the C–V plot is affected [24–27]. It is therefore important to include the effect of the frequency and series resistance and examine in detail the frequency dispersion of capacitance in the forward capacitance–voltage and conductance–voltage characteristics.

MS Schottky diodes formed by depositing various metals on the Si have been studied over a wide frequency range [7,22]. The values of the capacitance and conductance depend on various parameters, such as density of surface states, series resistance, insulator layer thickness and barrier height formation between metal and semiconductor. As explained above, in recent studies, some researches [22,27–29] have reported an anomalous peak in the forward bias (C–V) characteristics. Among these very interesting study is presented by Kılıçoğlu [19]. Chattopadhyay and Raychaudhuri [28] have been shown that, in the presence of a series resistance, the C–V characteristics should exhibit a peak. The peak value of the capacitance (C) and its position depends on a number of various parameters such as, doping concentration, series resistance of device, and the thickness of the interfacial insulator layer [27,30].

The various experimental works have been studied on Si crystals using different metals as rectification contact [4,8,9,12,15–22,30,31]. However, literature reports on the of frequency and voltage dependent electrical characteristics of Sn/p-Si (MS) Schottky structures using C–V and G/ω–V (in the frequency range of 50 kHz–1 MHz) measurements are rare. Therefore, in this study, we have investigated the frequency and voltage dependences of the electrical characteristics of Sn/p-Si (MS) Schottky diodes using C–V and G/ω–V measurements. To determine accurate values of R_S and N_{SS} of the Sn/p-Si Schottky diodes, we have applied the method by Nicollian and Brews [7]. Furthermore, the N_{SS} distribution profiles of Sn/p-Si Schottky diodes were obtained from the forward bias I–V dates as a function of frequency. Experimental results clearly show that both N_{SS} and R_S are important parameters that influence the electrical characteristics of MS structures.

2. Experimental procedure

The Sn/p-type Si Schottky (MS) diodes were fabricated on 2 in. diameter p-type single crystal silicon wafer with (1 0 0) surface orientation and 6.248 Ω cm resistivity. The wafer was chemically cleaned using the RCA cleaning procedure. The RCA cleaning procedure is the industry standard for removing contaminants from wafers. The RCA cleaning procedure has three major steps used sequentially: (i) organic clean: removal of insoluble organic contaminants with a 5:1:1 H_2O:H_2O_2:NH_4OH solution, (ii) oxide strip: removal of a thin silicon dioxide layer where metallic contaminants may accumulated as a result of (i), using a diluted 50:1 H_2O:HF solution, and (iii) ionic clean: removal of ionic and heavy metal atomic contaminants using a solution of 6:1:1 H_2O:H_2O_2:HCl. The procedure was also designed to prevent replanting of metal contaminants from solution back to the wafer's surface. When finished, the polished side should be seculars with no residue. The native oxide on the front surface of the substrate was removed in HF:H_2O (1:10) solution and finally the wafer were rinsed in de-ionized water for 30 s. Then, low resistivity ohmic contact to p-type Si (1 0 0) wafers was made by using Al, followed by a temperature treatment at 570 °C for 3 min in N_2 atmosphere. We have also used a RCA cleaning after Al deposition (back contact) for removal of Al contamination on the front side (also the native oxide) which may disturb the characteristics of the diode. The Schottky contacts were formed by evaporation of Sn dots with diameter of about 1.5 mm (diode area = 1.76×10^{-2} cm^2). All evaporation processes were carried out in a turbo molecular fitted vacuum coating unit at about 10^{-6} mbar.

The capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements were performed in the frequency range of 50 kHz–1 MHz by using a HP 4192A LF impedance analyzer (in the range of 5 Hz–13 MHz) and the test signal of 40 m $V_{rms.}$ All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card at room temperature in the dark.

3. Results and discussion

Conductance technique is based on the conductance losses resulting from the exchange of majority carriers between the interface states and majority carrier band of the semiconductor when a small ac signal is applied to the semiconductor structures [6]. The applied ac signal causes the Fermi level to oscillate about the mean positions governed by the bias dc bias, when the semiconductor device is in the depletion. The voltage dependent capacitance–frequency plots show the variation of the conductance in the depletion region for the same frequency interval, indicating the existence of different time-dependent responses of interface states. Thus, both C–V and G–V plots for high frequency (at ≈1 MHz) applied voltage (Figs. 1 and 2, respectively) became almost constant. As can be seen from Figs. 1 and 2, the capacitance (C_m) and conductance (G/ω) plots are dependent on both the bias voltage and frequency. The capacitance–voltage characteristics have an anomalous peak (−1.25 V) and the values of capacitance give a

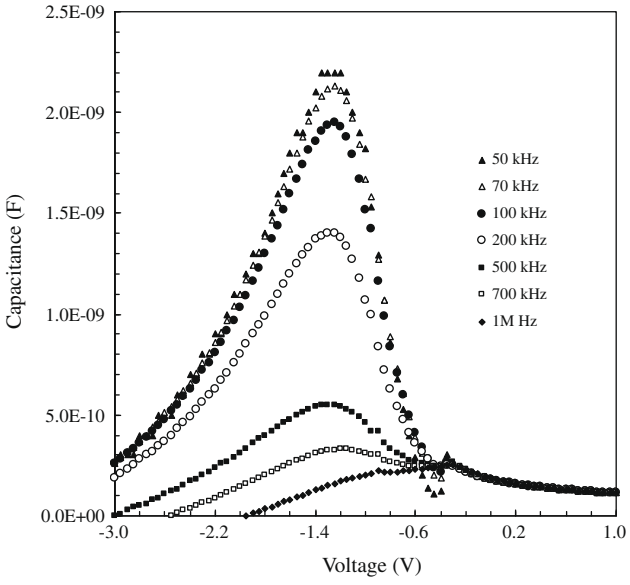

Fig. 1. The experimental capacitance–voltage characteristics of the Sn/p-Si (MS) Schottky structure in the frequency range 50 kHz–1 MHz.