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Design guidelines for the integration of Geiger-mode avalanche diodes in standard CMOS technologies

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ABSTRACT

The goal of this paper is to provide some useful design guidelines at the device level regarding the main challenges to be typically faced in the design and integration of Geiger-mode avalanche diodes in a standard CMOS process. Different techniques are found in literature in order to avoid premature edge breakdown with the aim of limiting the electric field at the edges to be weaker than in the multiplication region. In this article, the use of such techniques, the conditions where they can effectively work and above all their limitations are studied by means of TCAD simulations for various diode architectures. Additionally, the noise performance is discussed by focusing on the band-to-band tunneling and shallow trench isolation enhanced dark count rates. Geiger-mode bias techniques as well as a synthesis on the pros and cons of the various avalanche diode architectures are finally presented aiming at facilitating future design choices.

1. Introduction

Avalanche diodes operating in Geiger-mode have been extensively studied and implemented during the last decades in manifold research and commercial applications for the detection of weak optical signals in the visible and near-infrared spectrum range [1–3]. During the last few years active R&Ds have been studying the implementation of these devices in the field of High Energy Physics and Medical Physics for the detection of ionizing particles in tracking applications [4,5] opening a new promising path of application for this type of device. A Geiger-mode avalanche diode consists of a p–n junction which is reverse biased above the breakdown voltage so that a single electron–hole pair generated in the space charge region of the junction can trigger an avalanche process by impact ionization, giving rise to a macroscopic electrical signal [1–3]. In order to avoid any permanent damage on the device caused by the consequently high current density flowing through the diode, the breakdown process has to be quenched right after the avalanche has built-up. This is done thanks to a quenching element (e.g. a resistor) which has to promptly lower the voltage across the diode below the breakdown, interrupting in this way the avalanche multiplication process [1–3]. It is worth noting that despite of the small thickness of the sensitive material, i.e. the junction space charge region, a strong enough electrical signal is provided by the large charge amplification which overcomes the need of any analog amplification stage.

However there are several aspects which have to be carefully accounted for in the design of an avalanche diode operating in Geiger mode. These devices are indeed affected by dark counts, i.e. undesired avalanche events triggered by electron–hole pair generation processes in the diode space charge region. Dark count rate depends on the adopted CMOS process and increases with the sensor area as well as with temperature and excess bias. Dark counts can be divided into primary and secondary pulses [1]. Primary pulses are produced by Shockley–Read–Hall (SRH) and band-to-band tunneling generation processes. Conversely, secondary pulses, generally referred to as after-pulses, are avalanche events correlated to a previously occurred avalanche event. During an avalanche pulse, part of the carriers crossing the junction is indeed captured by deep levels in the diode space charge region and subsequently released with a statistically fluctuating delay, whose mean value depends on the involved deep levels. According to a probability that depends on the number of trapped carriers, a released carrier can then re-trigger an avalanche producing in this way a secondary pulse.

A Geiger-mode avalanche diode should have a uniformly distributed electric field in the active region [2,3], i.e. the region where the avalanche multiplication process occurs. Different techniques have

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been developed with the aim of limiting the electric field at the edges to be weaker than in the multiplication region [6–10] thus preventing Premature Edge Breakdown (PEB). The accomplishment of all these design requirements is particularly challenging when considering an integration in commercial standard CMOS technologies which does not allow a tailored design but conversely enables a cost-effective production of a complete detector based system, integrating the sensor together with the read-out electronics.

The goal of this paper is to provide some useful design guidelines at the device level regarding the main challenges to be typically faced in the design and integration of avalanche diodes in a standard CMOS process. The studies are conducted by means of TCAD simulations of several avalanche diode architectures implemented in a 130 nm standard CMOS process. In Section 2, these architectures will be presented with the aim of preventing premature edge breakdown effects. In Section 3, the noise performance of the architectures shown in Section 2 will be discussed by focusing on the Band-to-band (B2B) tunneling and Shallow Trench Isolation (STI) enhanced dark count rate (DCR). In Section 4, Geiger-mode bias techniques applied to the studied avalanche diode architectures will be shortly discussed. Finally in Section 5, a synthesis on the pros and cons of the various avalanche diode architectures with the aim of facilitating future design choices will be given.

2. Premature edge breakdown prevention

A simple p–n junction structure consisting for example of a n+ region over a p-type substrate (Fig. 1a) cannot be suitable for an avalanche diode because of the curvature at the device edge leading to a local higher electric field (Fig. 1b) and thus causing PEB [10].

In the present work, different PEB prevention techniques found in literature [6–10] have been studied and compared with TCAD simulations by implementing 2D Cylindrical geometries and adopting standard CMOS 130 nm process parameters. In the following subsections, the use of such techniques, the conditions where they can effectively work and their limitations are presented. Please note that CMOS processes below the 250 nm node feature shallow trenches filled with SiO_2 around p+ and n+ implantation areas to improve isolation. However, for the sake of clarity, in subsections 1, 2, 4, 5, the presence of Shallow Trench Isolations (STI) has not been considered. In a real case, STI can be prevented by adopting some proper process layers effectively acting as a "STI stop" layer.

2.1. Low doped guard ring

This technique consists in surrounding the p–n junction with a low doped guard ring, as depicted in Fig. 2a.

An implementation of such a structure in a 130 nm CMOS process is shown in Fig. 2b where the avalanche diode consists of a p+/n-well junction surrounded by a low doped p-well [3–5]. This layout may violate the design rules of a standard CMOS process as the intersection of diffusion and well regions, e.g. p+ diffusion and p-well, is generally not allowed. However foundries may allow to waive these rules. The effectiveness of this solution is shown in Fig. 3, where the electric field color map of the structure represented in Fig. 2b has been obtained by means of TCAD simulations. The avalanche model in the electrical device simulator has been switched off in order to study the electric field distribution before the occurrence of an avalanche event.

Thanks to a low doped p-well on the p+ diffusion edges the electric field can be successfully smoothed down since the field peak in the space charge region of a p–n junction decreases as the doping concentrations are reduced.

This topology has been adopted since the early stages of the Geiger-mode Avalanche Diode developments besides being one of the

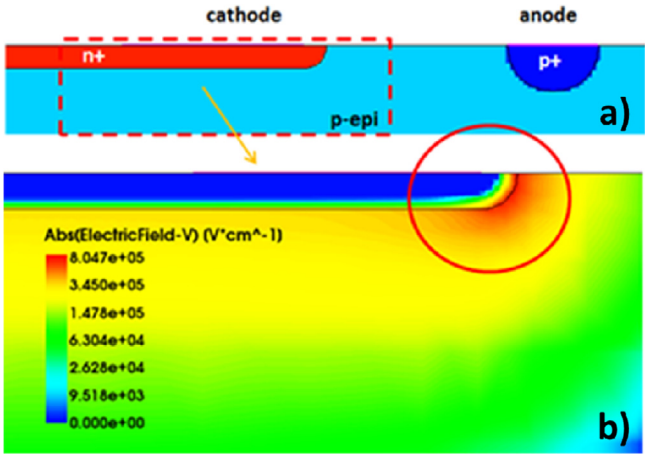

Fig. 1. (a) A uniformly doped n+/p- junction. (b) Electric Field Magnitude color map obtained with TCAD simulation. The field is maximal at the n+ region edges.

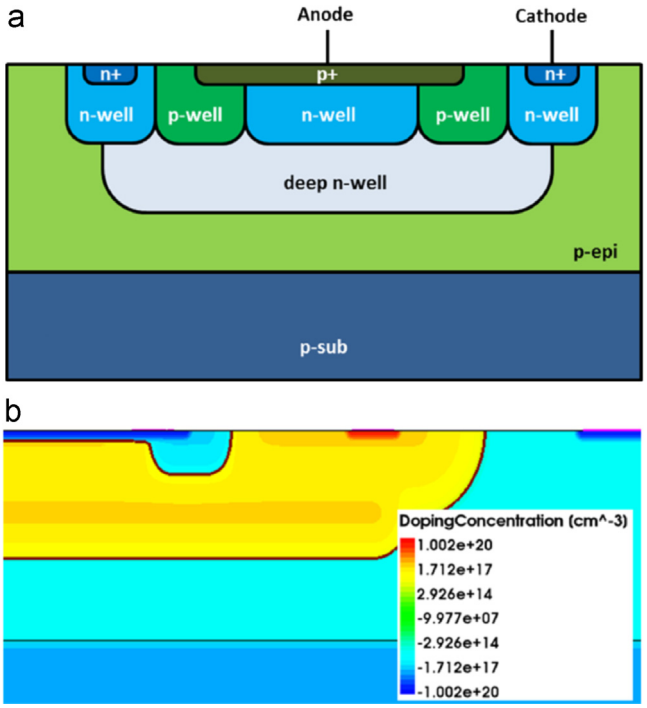

Fig. 2. p+/n-well diode surrounded by a p- guard ring (p-gr). (a) Schematic representation. (b) Effective doping concentration color map. NB: positive doping concentration values refer to n-type doping whereas negative one refers to p-type.

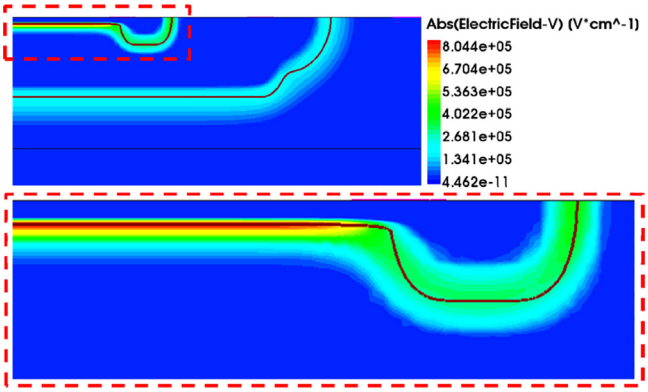

Fig. 3. Electric field color map of a p+/n-well diode surrounded by a p- guard ring (p-gr). $V_{rev} = 16.32$ V (simulated $V_{bd} = 11.66$ V).