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A low power low area capacitor array based Digital to Analog Converter architecture

A. Purushothaman [a,*], Chetan D. Parikh [b]

[a] Dhirubhai Ambani Institute of Information and Communication Technology, Gandhinagar, Gujarat, India
[b] International Institute of Information Technology, Bangalore, India

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ABSTRACT

This paper presents a capacitor based Digital to Analog Converter architecture, which gives comparable performance with the conventional architecture with approximately half the total capacitance. The proposed architecture reduces the area and power dissipation in comparison with the conventional scheme. Further to these advantages, the proposed DAC architecture does not demand an additional reference voltage or an additional switching circuit. Closed form formulas to estimate the standard deviation of INL, DNL and the power consumption are derived. A comparison is also made between the standard architectures and the proposed architecture for the same unit capacitor, in addition to analyzing the capacitor parasitics and mismatches. These analytical comparisons are validated by simulating the proposed architecture and all the other conventional architectures for 10 bits with UMC 180 nm CMOS technology.

1. Introduction

Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs) are integral parts of all communication systems. Past research on data converters had focused on reducing power and area, while increasing the speed. Of late, capacitor array DACs have become more attractive in low power applications such as bio-medical applications and sensor networks. On the contrary, the conventional capacitor array architecture consumes more switching energy and settling time for high resolution applications. Many techniques have been described to reduce the switching energy and settling time, though they were not successful in meeting all the required criteria. For example, different switching schemes [1–3] have been used to reduce power consumption, but compromises on speed and area. A charge sharing scheme [11] reduced the switching energy, but it also decreased the frequency of operation. On the other hand, the split capacitor array [4–6] was able to reduce the switching energy as well as increase the speed. Multi-step binary weighted capacitor array DAC [7] increased the speed while sacrificing the area. In [8], radix3/radix2 search algorithms were used to improve the convergence speed. Some researches proposed layout techniques [9,10] that could reduce the parasitic capacitances, thus improving the performance of the DAC.

In this paper, we have proposed an architecture that is capable of reducing the total capacitance, thereby decreasing area and power dissipation. The rest of the paper is organized as follows. Section 2 introduces the proposed architecture. Section 3 derives the closed form equations for standard deviation of Integral Non Linearity (INL), Differential Non Linearity (DNL) and power dissipation. Section 4 provides a comprehensive comparison between the proposed architecture and three commonly used architectures. Section 5 presents a detailed analysis of capacitor parasitics and capacitor mismatches. Finally, the last section concludes the paper.

2. The proposed capacitor array DAC

The conventional capacitor array DAC consists of an array of individually switched binary weighted capacitors with a total capacitance of $2^N C_0$ for converting an N-bit digital input into its equivalent analog value, where C_0 is the unit capacitance value. This architecture has limited use for higher resolution due to the larger capacitor ratio evaluated from Most Significant Bit (MSB) capacitor to Least Significant Bit (LSB) capacitor. The MSB capacitor, which is $2^{N-1} C_0$ decides the power, area and settling time.

* Corresponding author.
E-mail addresses: ampurushothaman@gmail.com (A. Purushothaman), parikh_chetan@yahoo.com (C.D. Parikh).

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Eliminating the MSB capacitor enhances the performance of the DAC almost to double. The proposed architecture performs the function of MSB capacitor with three unit capacitors.

An N-bit DAC has (2^N-1) discrete output levels. To convert an N-bit DAC to $(N+1)$ bit DAC, an MSB capacitor that could add another 2^N output levels should be introduced. Thus, the total output levels reach $(2^{N+1}-1)$. These added output levels are considered significant only if the LSB is one. The output levels when the LSB is zero are same as the output levels generated by an N-bit DAC.

For an $(N+1)$ digital to analog conversion, the proposed method uses the conventional conversion principle by using an N-bit DAC when LSB is zero. When LSB is one, it utilizes three unit capacitors to generate the remaining output levels. This proposed method neither creates a $V_{ref}/2$ nor halves the unit capacitor, but keeps the settling time the same, while power and area are almost reduced. Since it employs series capacitors, the linearity is compromised, but it is comparable with the conventional DAC.

To illustrate the working of the proposed DAC architecture further, a 4-bit DAC which is shown in Fig. 1 is taken as an example. Conventional single ended 4-bit DAC produces 15 output discrete levels $\sum_{m=1}^{15} mV_{ref}/16$, in these, seven discrete levels $\sum_{m=1}^{7} 2mV_{ref}/16$ (corresponds to the input digital sequences with LSB=0) can be generated by conventional 3-bit DAC. The proposed DAC acts as a 3-bit DAC when switches S_d and S_{d1} are open and the bottom plate of capacitor C_1 is connected to V_{SS}. Switches S_d and S_{d1} are controlled by the LSB bit. When LSB=1, switches S_d and S_{d1} are closed. The bottom plates of C_1 and C_2 are connected to V_1. The equivalent circuit of the proposed scheme for this configuration is shown in Fig. 2. From Fig. 2, V_x can be derived as

$$V_x = V_{ref}(2m+lm+l)/(2(m+l+k)+l(m+k)) \tag{1}$$

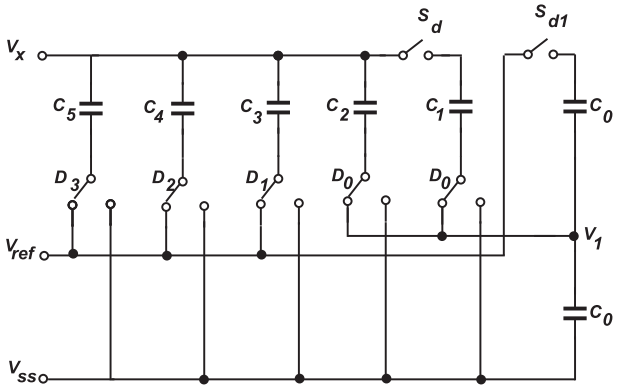

Fig. 1. 4-bit DAC schematic.

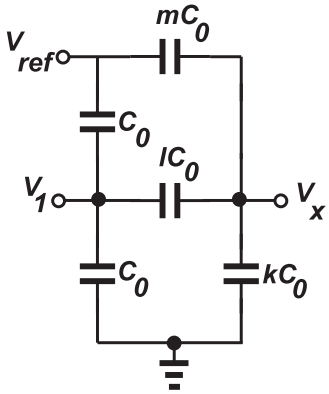

Fig. 2. Generalized equivalent circuit for any bit pattern.

Where m is the sum of capacitances with bottom plates connected to V_{ref}

$$m = 2^{N-2}D_{N-1} + 2^{N-3}D_{N-2} + \cdots + D_1 \tag{2}$$

The capacitors with bottom plates connected to ground are summed up as k and is given as

$$k = 2^{N-2}\overline{D}_{N-1} + 2^{N-3}\overline{D}_{N-2} + \cdots + \overline{D}_1 + \overline{D}_0\overline{S_d} \tag{3}$$

and

$$l = D_0 + D_0 S_d \tag{4}$$

where n is the number of bits, $D_{n-1}\ldots D_0$ are the digital inputs, $\overline{D}_{n-1}\ldots\overline{D}_0$ are their complements.

By substituting the values of m, k and l in Eq. (2), Eq. (2) can be rewritten as

$$V_x = \left(\frac{2^{N-2}D_{N-1} + 2^{N-3}D_{N-2}\ldots D_1}{2^{N-1}}\right)V_{ref} + \left(\frac{D_0}{2^{N-1}(1+D_0)}\right)V_{ref} \tag{5}$$

Eq. (5) ensures that all the necessary output levels are generated. When LSB=0, output levels depend on the first term and the second term is used when LSB=1 and generates the extra voltage required.

3. Closed form formulas for standard deviation of INL, DNL and power consumption

The closed form expressions to evaluate the standard deviation of INL, DNL and power consumption are derived in this section. These derivations provide justification for the proposed architecture. The closed form formula for the standard deviation of INL, DNL and the power consumption for Conventional Binary Weighted (CBW) DAC, Binary Weighted Capacitor array with attenuation Capacitor (BWA) and Split Binary Weighted Capacitor Array (SBW) are derived in [4,12]. The same procedure is used to derive the above said parameters for the proposed architecture which is supported by the simulation results in Section 4.

3.1. Derivation for standard deviation of INL

It is assumed that all the errors are in the unit capacitors. The values of the unit capacitor are random variables which are independent identically distributed Gaussian in nature. Each individual capacitor is modeled as the sum of the nominal capacitance plus the error [4].

$$C_N = 2^{N-2}C_0 + \delta_N \tag{6}$$

$$C_{N-1} = 2^{N-3}C_0 + \delta_{N-1} \tag{7}$$

$$C_{01} = C_0 + \delta_0 \tag{8}$$

Where C_{01} is the unit capacitor with the error. The error term $=\delta_N$ has zero mean and a standard deviation of [3]

$$E[\delta_N^2] = 2^{N-2}\sigma_0^2 \tag{9}$$

where σ_0^2 is the unit capacitor's standard deviation. If there are no initial charges, then V_x can be expressed as

$$V_x = \left(\frac{\sum_{k=2}^{N} 2^{(k-2)}C_0 D_{k-1}}{2^{(N-1)}C_0} + \frac{C_0 D_0}{2^{(N-1)}(C_0 + C_0 D_0)}\right)V_{ref} \tag{10}$$