Microelectronics Journal 46 (2015) 988–995

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A 10-bit 300-MS/s asynchronous SAR ADC with strategy of optimizing settling time for capacitive DAC in 65 nm CMOS

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ARTICLE INFO

Article history:
Received 24 October 2014
Received in revised form
11 March 2015
Accepted 21 August 2015
Available online 5 September 2015

Keywords:
SAR ADC
Low power
High speed
Settling time
Asynchronous

ABSTRACT

A 10-bit 300-MS/s asynchronous SAR ADC in 65 nm CMOS is presented in this paper. To achieve low power, binary-weighed capacitive DAC is employed without any digital correction or calibration. Consequently, settling time for the capacitive DAC would be a dominant limiting factor for the ADC operating speed. A novel architecture is proposed to optimize the settling time for the capacitive DAC, which depends merely on the on-resistance of switches and the capacitance of unit capacitor and irrelevant to the resolution. Therefore, high-speed high-resolution SAR ADC is possible. What is deserved to highlight is that the architecture improves the ADC performance at a fraction of the cost, with only some capacitors and control logic added. Post-layout simulation has been made for the SAR ADC. At a 1.2-V supply voltage and a sampling rate of 300 MS/s, it consumes 1.27 mW and achieves an SNDR of 60 dB, an SFDR of 67.5 dB, with the Nyquist input. The SAR ADC occupies a core area of $450 \times 380\ \mu m^2$.

1. Introduction

With the feature size of CMOS devices scaled down, SAR ADC is going mainstream as the feature size of CMOS devices scales down. Its distinctive characteristics are simple structure, high energy-efficiency and outstanding compatibility with the digital process. SAR ADC, requiring several comparison cycles to complete one conversion, generally has limited operational speed. In recent years, many experts are dedicating to improving the operational speed for SAR ADC [1–4]. Time-interleaved SAR ADC proposed in [1] requires harsh clock accuracy since Signal-to-noise ratio (SNR) is destructible by clock jitter. Flash-SAR ADC proposed in [2] would introduce static power due to flash ADC. Resistors, of which the mismatch property is poorer, are also used in this architecture. In addition, more than one comparator is employed. Since offset still exists among the comparator offset voltages, offset canceling for the comparator would be of the essence. Pipeline-SAR ADC proposed in [3,4] can realize both high-speed and relatively low-power specifications by reducing the number of op-amps. Nevertheless, the requirement of interstage gain in the architecture still requires at least one op-amp. This will not only consume static power, but also set limitations to compatibility with system-on-chip (SOC) under low supply voltage condition. With this proposed strategy, the settling time of the DAC can be reduced significantly to improve the operation speed, while only SAR ADC topology and one comparator are required. Moreover, the settling time is insensitive to the resolution, making possible the high-speed high-precision SAR. Employed the proposed architecture, a 1.2-V 10-bit 300-MS/s SAR ADC is designed in 65 nm CMOS technology. Post-layout simulation shows that at a 300 MS/s sampling rate, the ADC achieves an ENOB of 9.67 bits and consumes 1.27 mW with the Nyquist input, resulting in a FOM of 5.2 fJ/conversion-step.

2. Architecture design

Since the SAR search algorithm resolves a single bit on each clock cycle, it is difficult to simultaneously increase both resolution and throughput. During one conversion, most of the time is occupied by DAC settling time, comparator decision time and reset time. With the circuit structure described in [5], the comparator decision time and reset time can reach 100 ps and 80 ps, respectively. Consequently, DAC settling time becomes the major limiting factor. In this paper, a novel strategy to improve the settling time is proposed.

To illustrate the proposed strategy, case of 4-bit resolution is taken as an example. As shown in Fig. 1, the whole DAC is comprised of three sub-DACs. The most significant two bits are obtained by Sub-DAC1, while the other sub-DACs contribute to only one bit. Top-plates sampling is employed to save half the capacitors. In the sampling phase, switches S_T are closed and input signals, V_{IP} and V_{IN}, are sampled on the top-plates of capacitors. All the bottom-plates of capacitors are initially loaded with the

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http://dx.doi.org/10.1016/j.mejo.2015.08.008
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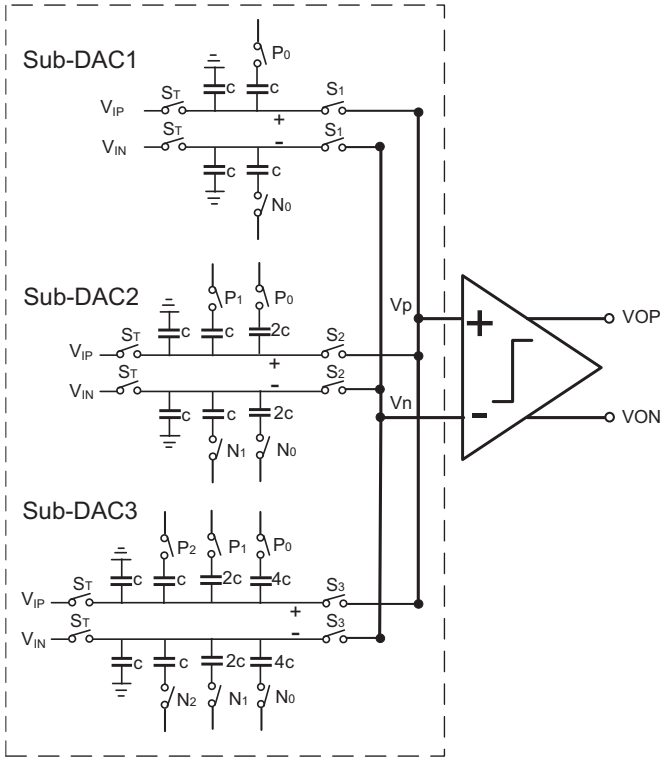

Fig. 1. Proposed topology for 4-bit SAR ADC.

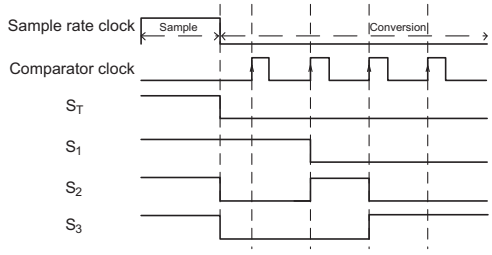

Fig. 2. Switching scheme for S_T, S_1, S_2, S_3 and comparator clock.

sequence of '0000'. Subsequently, the comparison phase arrives. Switching sequences for S_T, S_1, S_2, and S_3 are shown in Fig. 2, and comparator clock is generated by asynchronous control logic to achieve high speed goal. On arrival of the falling edge of the sample rate clock, S_T, S_2, and S_3 are switched off, and only S_1 is still on. In a situation like this, no sub-DACs except for sub-DAC1 is connected to comparator for conversion. On account of top-plates sampling, the MSB can be obtained the moment the first rising edge of the comparator clock arrives, with no capacitor switched. According to the MSB, either P_0 or N_0, would be switched from '0' to '1'. For example, if MSB=0, all switches P_0 belonging to sub-DAC1, sub-DAC2, sub-DAC3 would be switched from '0' to '1'. Then voltages across capacitors in all sub-DACs begin to re-established, but only settling of sub-DAC1 influences the second bit, which is obtained once the second rising edge of the comparator clock arrives. Since in sub-DAC1, the switched capacitor for the second bit is equal to unit capacitor, the course of settling can be completed soon. After the second comparison, clk1 is activated, so that S_1 is turned off and S_2 is closed to connect sub-DAC2 to the comparator. Meanwhile, according to the refreshed comparator result, P_1 or N_1 would be switched in the similar way. Note that there should be enough time for the voltage across capacitors in sub-DAC2, resulting from both P_0/N_0 and P_1/N_1, to establish well before the third rising edge of comparator coming. With regard to the following comparisons, operations are done similarly.

Assuming the on-resistance of switches connecting bottom-plates of capacitors to either '0' or'1' to be Ron, time-constants for each capacitor in the sub-DACs are listed in Table 1.

Architecture for the proposed SAR with resolution being 4-bit is shown in Fig.3. The decision time for comparator is represented by t_{comp} and the delay time from comparator outputs to DAC is represented by t_{delay}.

Let the period of comparator clock be T_{comp}, the maximum settling time for DAC within each comparison cycle can be expressed as:

$$t_{DAC} = T_{comp} - t_{comp} - t_{delay} \tag{1}$$

If a switch (on-resistance equals R_{on}) connects the corresponding capacitor (capacitance equals C) from '0' to '1', the time required for the voltage across the capacitor to settle sufficiently to 99% of the final value can be calculated from the following expression, where V_{final} represents the final value across the capacitor, and τ is equal to R_{on} times C.

$$0.99V_{final} = V_{final}(1 - e^{-\frac{t}{\tau}}) \tag{2}$$

The required settling time t can be calculated from (2) to be 4.6τ. As a consequence, the following formulas must be satisfied, so that the settling for each capacitor can be guaranteed.

$$\begin{cases} 4.6 \times \tau_{13} \le t_{DAC} \\ 4.6 \times \tau_{22} \le t_{DAC} \\ 4.6 \times \tau_{31} \le t_{DAC} \\ 4.6 \times \tau_{23} \le T_{comp} + t_{DAC} \\ 4.6 \times \tau_{32} \le T_{comp} + t_{DAC} \\ 4.6 \times \tau_{33} \le 2T_{comp} + t_{DAC} \end{cases} \tag{3}$$

Substituting data in Table 1 into (3), (3) can be rewritten as

$$\begin{cases} 4.6 \times \frac{1}{2}R_{on}C \le t_{DAC} \\ 4.6 \times \frac{3}{4}R_{on}C \le t_{DAC} \\ 4.6 \times \frac{7}{8}R_{on}C \le t_{DAC} \\ 4.6 \times R_{on}C \le T_{comp} + t_{DAC} \\ 4.6 \times \frac{3}{2}R_{on}C \le T_{comp} + t_{DAC} \\ 4.6 \times 2R_{on}C \le 2T_{comp} + t_{DAC} \end{cases} \tag{4}$$

Since $t_{DAC} < T_{comp}$ holds true, which can be deduced according to (1), one can found that (4) can be simplified just by the inequality relevant to τ_{31}. That is:

$$4.6 \times \frac{7}{8}R_{on}C \le t_{DAC} \tag{5}$$

T_{comp}, t_{delay} and t_{DAC} can be adjusted by the logic delay, separately, while t_{comp} is approximately 200 ps, as is mentioned above.

By this analogy, the conclusion for N-bit resolution can be drawn in the similar way. The only restriction for settling occurs when the LSB

Table 1
Time-constant relevant to each capacitor for 4-bit SAR ADC.

τ	P_2/N_2	P_1/N_1	P_0/N_0
Sub-DAC1	×	×	$\tau_{13}=1/2\ R_{on}C$
Sub-DAC2	×	$\tau_{22}=3/4R_{on}C$	$\tau_{23}=R_{on}C$
Sub-DAC3	$\tau_{31}=7/8R_{on}C$	$\tau_{32}=3/2R_{on}C$	$\tau_{33}=2R_{on}C$