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Physical phenomena affecting performance and reliability of 4H–SiC bipolar junction transistors

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ABSTRACT

The silicon carbide bipolar junction transistor (BJT) is attractive for use in high-voltage switching applications offering high-voltage blocking characteristics, low switching losses, and is capable of operating at current densities exceeding 300 A/cm^2. However, performance reliability issues such as degradation of current gain and on-resistance currently prohibit commercial production of 4H–SiC BJTs. This paper examines the physical mechanisms responsible for this degradation as well as the impact that these physical phenomena have on device performance. Results were obtained through the examination of several types of N–P–N BJT structures using various fabrication methodologies. Electron-beam induced current (EBIC) and potassium hydroxide (KOH) etching were used to characterize defect content in the material, before and after device current stress, when possible. It was found that Shockley stacking faults (stress-induced structures) associated with the forward voltage drift phenomenon in SiC bipolar diodes, also play a major role in the reduction of gain and an increase of on-resistance of the BJTs. However, results from some devices suggest that additional processes at the device periphery (edge of the emitter) may also contribute to degradation in electrical performance. Hence, it is essential that the sources of electrical degradation, identified in this paper, be eliminated for SiC BJTs to be viable for commercial scale production.

1. Introduction

SiC is an attractive material for use in high power devices. Its wide-bandgap, low intrinsic carrier concentration, and high thermal conductivity make it suitable for high-voltage, high power-density applications. Power switches such as JFETs, MOSFETs, BJTs, IGBTs, GTOs, etc. have been demonstrated for different applications [1–12]. Among these devices, SiC BJTs offer numerous benefits in high power systems due to their unique properties such as low on-resistance, normally-off, positive temperature coefficient of the resistance, and fast switching speed [8,13–15]. One major challenge for the commercialization of SiC power BJTs is performance degradation in both on-resistance and current gain. Two possible mechanisms, which may be simultaneously present in the device, are thought to be responsible for the degradation: (a) increase of the density of surface states along the SiC/SiO_2 interface, which results in an increased surface recombination current [16,17] and (b) bulk recombination in the base due to the generation and growth of Shockley stacking faults (SSFs) [17,18]. Although the later mechanism is similar to the degradation of 4H–SiC p–n junction diodes associated with the appearance of SSFs in the entire base region of the diode [19–21], no clear experimental proof of this mechanism was provided in the case of 4H–SiC BJTs.

The objective of the current work is to characterize the degradation phenomena observed in 4H–SiC bipolar junction transistors as it pertains to device reliability. This paper shows that when nucleation sites are available, development of SSF by glide of Shockley partial dislocations in the basal plane, is a key contributor to performance degradation in SiC BJTs. Electron-beam induced current (EBIC) is used to reveal the presence of basal plane dislocations (BPDs) within the collector-base junction of the devices after they have been subjected to current stress in the common emitter configuration. Our results also suggest that, in the absence of SSFs, other phenomena exist that can degrade the performance of these devices when operated at high current densities.

2. Experiment

Cross sections of two device types used in the experiments are shown in Fig. 1. Large area device structures (Fig. 1a) were used in order to examine the impact of subsurface features such as BPDs in

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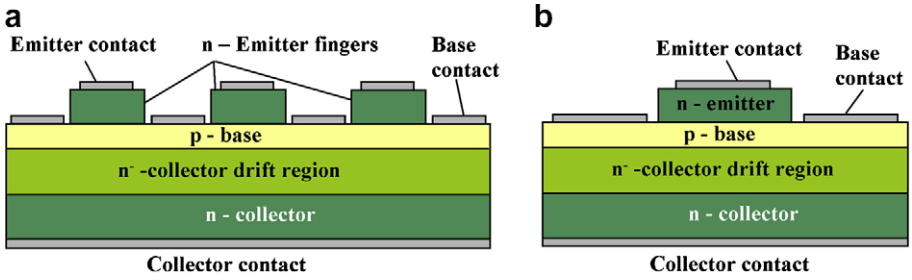

Fig. 1. Cross sections of the devices used in the experiments. (a) Large area finger-type device structure and (b) continuous device structure.

the vicinity of the collector-base junction of the devices. These devices (referred further as Device 1 to Device 3) were of an interpenetrating finger design having a 10 μm emitter finger width with a 12.5 μm pitch. Additional structures (Fig. 1b) were used in order to facilitate characterization of the emitter-base junction. These were continuous structures, not of the finger type. All devices were fabricated on 8° off (0001) 4H–SiC substrates by Cree Inc. Dies were produced on epilayers containing BPDs as well as epilayers produced by a BPD-free epitaxial growth process [22]. Multiple devices were fabricated on each die. Active area dimensions of each device measure 1.5 mm × 1.5 mm. The collector drift region of all devices was 14 μm thick n-type, doped to 4.8×10^{15} cm^{-3}. The base formation was accomplished using epitaxial growth for Device 1 and ion implantation for Device 2, Device 3, and non-finger-type devices. The base thickness was 1 μm for all devices. The base doping concentration was about 2×10^{17} cm^{-3} for Devices 1 and 3, and about 5.5×10^{17} cm^{-3} for Device 3, and non-finger-type devices. The large area finger structure device dies, each containing 4 device structures, were packaged prior to electrical characterization. Only a single device from each die was stressed and characterized. Initial, pre-stress I_C–V_{CE} curve families as well as the base-emitter junction I–V curves were obtained from each device. Devices 1–3 were subjected to 2 h of electrical stress in the saturation region of operation using a collector current of 3 A (130 A/cm^2) at room temperature. The above noted characterization measurements were then repeated after stress.

Device dies were removed from packaging in preparation for material characterization. All contact metals and oxides were removed chemically from each die prior to potassium hydroxide etching. KOH etching was performed for 3 min at 600 °C. There was a markedly obvious higher density of BPD-related pits in the degraded structure compared to the non-stressed devices and unused area on the same die. The BPD density in non-stressed devices and unused area of the die was obtained and further considered as initial BPD density for the stressed device from the same die assuming uniform distribution of BPDs before stress in each die. It should be noted that BPD etch pits observed in unused die area as well as in unstressed devices are most likely due to perfect BPDs. By contrast, in a stressed device this pit geometry may also be attributed to the 30° and 60° dissociated partial dislocations bounding SSFs in addition to any 0° perfect BPDs, like those observed in unused areas. If the initial BPD pit density estimates had been obtained from the stressed device area, the data would erroneously include pits due to the 30° and 60° partial dislocations. Subsequent to KOH etching, EBIC images were obtained from the collector-base junction of the degraded devices. The EBIC probe contact was made to the p-type base region of the devices. Sufficiently ohmic and low resistance probe contact is achievable despite removal of the base metallization. In this way, EBIC reveals electrically active subsurface defect content within a diffusion length of the base-collector p–n junction. The physical locations of BPDs and SSFs observed using EBIC may be compared with locations of etch-pits produced by KOH etching.

Additional device structures were characterized in a similar fashion with a few exceptions. The smaller non-finger type structures were not packaged prior to electrical measurement. Electrical measurements and stress were performed using probe contacts to the base and emitter metals while electrical contact to the collector was made by way of silver-paste to the probe stage. Electric stress was applied to the devices in the form of base-emitter forward current, with the collector contact floating. Several intervals of stress were applied to each tested device, with increasing current density in each stage. Following each stage of stress, the device junction and transistor I–V curves were obtained. Following electrical stress and characterization, all metals and overlayers were removed except for the base and emitter ohmic contact metal in order to obtain higher EBIC resolution. The ohmic metal was removed prior to KOH etching.

3. Results and discussion

The experimental results obtained from the large finger structure devices shows the development of SSFs as a result of electrical stress. The severity of degradation in the electrical performance is dependant on the size of the total faulted area in the stressed device and hence it is dependant on the number of nucleation sites available within the device structure. From the SiC p–n diode forward voltage drift studies, it is well established that BPDs serve as SSF nucleation sites. We demonstrate a correlation between the total faulted area after stress and the initial BPD density using three selected devices of varying initial BPD density. These selected Devices 1–3 have respective initial BPD densities of 1080 cm^{-2}, 155 cm^{-2}, and zero measured using KOH etching. These initial BPD density estimates were obtained using unused die area, outside the area of the stressed devices, in order to eliminate the possible count of partial dislocations bounding the stacking faults. Device 3 was produced using a BPD free epitaxial growth technique [22]. EBIC images of typical regions within the device active area for these three devices shown in Fig. 2 indicate that there is in fact a direct correlation between BPD density and fault affected area of the devices after stress.

Fig. 3 shows the I_C–V_{CE} curves obtained before and after stress from these three devices and Table 1 summarizes the electrical characterization results. In Table 1, V_{fBE} refers to the base-emitter voltage at 100 A/cm^2 collector current density, V_A (a measure of device ideality) refers to the Early voltage which was defined as the voltage at the intersection of the straight-line extensions of the active-region collector characteristics with V_{CE} axis, R_{ON} refers to the device specific on-resistance, and β refers to the current gain. Note that the pre-stress β of Device 1 is higher than the β of Devices 2 and 3, which is believed to be caused by differences in the emitter mesa structure height and shape. It is evident that the performance degradation reduces in severity with the reduction in fault affected area based on the electrical results shown in Fig. 3. As noted from Table 1, the generation of large number of SSFs in Device 1 corre-