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A single-bit sampling demodulator for biomedical implants

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ABSTRACT

A phase-shift keying (PSK) demodulator is demonstrated for the target application of low power and high data rate inductive links. The demodulator based on the single-bit sampling demodulation scheme is capable of operating in binary, quadrature, 8-, and 16-PSK mode. The prototype chip realized in 0.18-μm CMOS process can demodulate up to 1.25 MSymbol/s at 5-MHz carrier frequency. It occupies $240 \times 310\ \mu m^2$ and consumes 140 μA from 1.2 V.

1. Introduction

There are great interests for biomedical devices that can be implanted inside the human body such as retinal implant, cochlear implant, sphincter sensor, glaucoma sensor, intracranial pressure sensor system, functional electrical stimulation systems, and activity monitor and laboratory system [1]. Many of these devices need links to the external world for power delivery as well as data communication. For example, a retinal prosthesis continuously transmits video streaming data and a large amount of power in order to stimulate optic nerves using many electrodes [2,3]. In such an application, wireless power transmission is an attractive solution.

In order to avoid any damage to human body by power delivering, 1–10 MHz is often used since this frequency range has the least amount of absorption in skin [4]. Inductive links are widely used in this band. While power and data can be transferred through separate links for efficient power transmission [3,4,7,11,12], a single link transferring data and power simultaneously offers a simpler structure [2,5,8,10], which is of great advantage for implantation applications. Fig. 1 shows a block diagram for an inductive link composed of two magnetically coupled coils across skin. Both external and implanted units have data modulation and recovery blocks while only the implanted unit includes power recovery block. To transmit data and power simultaneously downlink (from the external unit to the implanted device), constant-amplitude modulation schemes such as pulse-width modulation [2], frequency-shift keying (FSK) [5–7] and phase-shift keying (PSK) [8–11] are often used since they are compatible with rectifier-based power recovery [8].

In most inductive-link transmitters and receivers reported so far, low-order modulation schemes such as amplitude-shift keying, FSK, binary phase-shift keying (BPSK) and quadrature phase-shift keying (QPSK) have been used. However, in applications where power and data are transmitted through the same coil, the available bandwidth is limited due to the power transfer efficiency consideration. Consequently, high-order modulation schemes that can enhance the total data rate without requiring more bandwidth is highly desirable. However, the conventional high-order demodulation techniques that are commonly used in communication systems cannot be adapted for implantation applications since they require a significant amount of power consumption.

We have previously demonstrated single-bit-sampling-based BPSK and QPSK demodulator for high-speed data communication applications [13–15]. In this paper, we extend our demodulation scheme so that it can be used for bio implantation applications with high spectral efficiency and lower power consumption. Our prototype demodulator, fabricated in TSMC 0.18-μm CMOS, can successfully demodulate 1.25-Mb/s binary, quadrature, 8-, and 16-PSK data using 5-MHz carrier frequency.

This paper is organized as follows. Section 2 explains our demodulation scheme based on the constellation diagram, and Section 3 describes implementation of the prototype chip. Section 4 gives measurement results and conclusion is given in Section 5.

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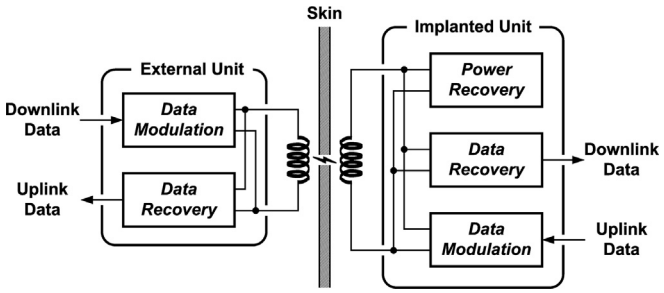
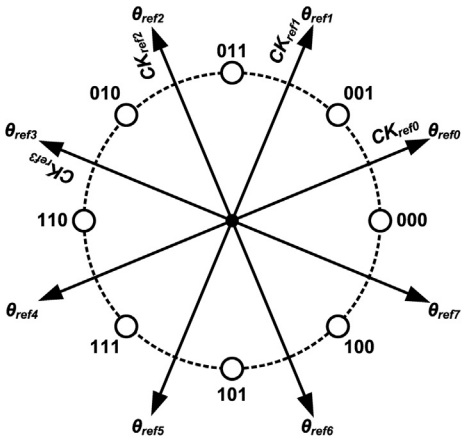


Fig. 1. Inductive link.

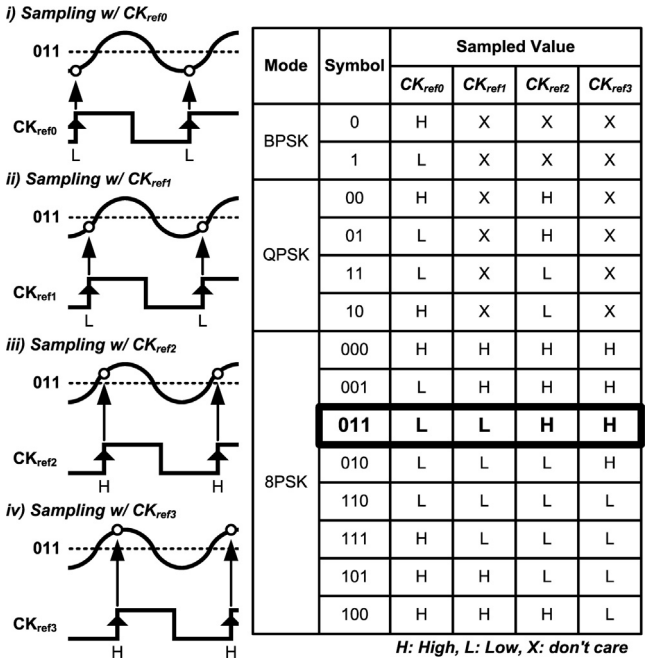


Symbol	Sign of (θ_{input} - $\theta_{ref\,n}$)							
	θ_{ref0}	θ_{ref1}	θ_{ref2}	θ_{ref3}	θ_{ref4}	θ_{ref5}	θ_{ref6}	θ_{ref7}
000	-	-	-	-	+	+	+	+
001	+	-	-	-	-	+	+	+
011	+	+	-	-	-	-	+	+
010	+	+	+	-	-	-	-	+
110	+	+	+	+	-	-	-	-
111	-	+	+	+	+	-	-	-
101	-	-	+	+	+	+	-	-
100	-	-	-	+	+	+	+	-

Fig. 2. Constellation of 8-PSK symbols and reference phases.

2. Single-bit sampling demodulation

Fig. 2 shows constellation of 8-PSK symbols represented by circles and reference phases by arrows ($\theta_{ref\,0-7}$). The phase of any input symbol can be determined by comparing input symbol phase with each of 8 reference phases. The phase comparison can be done by determining the sign of the phase difference between input symbol and each reference, or $\theta_{input}-\theta_{ref\,n}$. Fig. 2 shows the comparison result for each symbol in 8-PSK. This function can be realized in time domain by sampling input with multi-phase clock signals having reference phases. For example, if signs of $\theta_{input}-\theta_{ref\,n}$ are positive for $n=0, 1, 6, 7$ and negative for $n=2, 3, 4, 5$, then the input symbol is determined as 011. Since the result of phase comparison with $\theta_{ref\,4-7}$ is simply inversion of that with $\theta_{ref\,0-3}$ as shown in Fig. 2, only half of the reference phases, or multi-phase clocks, are needed in implementation. Fig. 3 shows timing diagrams for input symbol 011 with 4 multi-phase clock signals, $CK_{ref\,0-3}$. $CK_{ref\,0}$ and $CK_{ref\,1}$ produce sampled values of low, and $CK_{ref\,2}$ and $CK_{ref\,3}$ high. For each symbol of 8-PSK, sampled values are given in Fig. 3. Demodulation is complete when sampled values, LLHH, are decoded into the corresponding symbol, 011. Compared with conventional high-order PSK demodulation schemes based on multi-bit sampling analog-to-digital conversion



Mode	Symbol	Sampled Value			
		CK_{ref0}	CK_{ref1}	CK_{ref2}	CK_{ref3}
BPSK	0	H	X	X	X
	1	L	X	X	X
QPSK	00	H	X	H	X
	01	L	X	H	X
	11	L	X	L	X
	10	H	X	L	X
8PSK	000	H	H	H	H
	001	L	H	H	H
	011	**L**	**L**	**H**	**H**
	010	L	L	L	H
	110	L	L	L	L
	111	H	L	L	L
	101	H	H	L	L
	100	H	H	H	L

H: High, L: Low, X: don't care

Fig. 3. Timing diagrams of single-bit sampling (for input symbol 011).

and complex digital signal processing [16,17], our scheme consumes less power because it uses only single-bit samplers and simple phase comparison. In addition, since 8-PSK demodulator includes reference phases required for BPSK and QPSK, the demodulator operation mode can be easily changed when necessary using the decoding table given in Fig. 3. Since single-bit sampling is limited by the timing margin not by the amplitude, jitters on multi-phase clocks increase BER. In our proto-type chip, 16-PSK operation is implemented by doubling multiple phase clocks.

3. Implementation

Fig. 4a shows the block diagram of our prototype demodulator fabricated in TSMC 0.18-μm RF CMOS process. The receiver uses differential signaling to avoid 2nd-order distortions and achieve supply-noise immunity. The input signal is single-bit sampled by multiphase clocks generated from voltage-controlled oscillator (VCO). Sampled data are processed in the digital domain for symbol detection and phase extraction. The phase and frequency detector (PFD) unit offers up or down signal to the charge pump so that VCO phase is synchronized to the input signal for coherent operation. Compared to demodulators previously reported in [13–15], the demodulator in this work includes a CDR circuit, which rejects any ISI. Clock and data recovery (CDR) is employed to reject any inter-symbol interference (ISI) and provide clock synchronized to recovered data. The PSK decoder can be switched into BPSK, QPSK, 8-PSK or 16-PSK mode by an external control, and produces demodulated symbols as parallel data streams. CDR, PSK decoder and PFD unit are all implemented with auto placement and routing of standard logic cells. The core supply voltage for the prototype chip is lowered to 1.2 V using an internal supply regulator in order to reduce power consumption. For output and control signals, I/O and electrostatic discharge protection circuits are implemented using 3.3-V supply. Details of circuit implementation are given in Sections 3.1, 3.2 and 3.3. Fig. 4b shows the die photograph. The chip occupies 310 μm × 240 μm. Our target is 1.25-MSymbol/s symbol rate with 5-MHz carrier frequency.