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A fully integrated analog front-end circuit for 13.56 MHz passive RFID tags in conformance with ISO/IEC 18000-3 protocol

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ABSTRACT

A fully integrated analog front-end circuit for 13.56 MHz passive RFID tags is presented in this paper. The design of the RF analog front-end and digital control is based on ISO/IEC 18000-3 MODE 1 protocol. This paper mainly focuses on RF analog front-end circuits. In order to supply voltage for the whole tag chip, a high efficiency power management circuit with a rather wide input range is proposed by utilizing 15.5 V high voltage MOS transistors. Furthermore, a high sensitivity, low power consumption 10% ASK demodulator with a subthreshold-mode hysteresis comparator is introduced for reader-to-tag communication. The tag chip is fabricated in 0.18-μm 2-poly 5-metal mixed signal CMOS technology with EEPROM process. An on-chip 1 kb EEPROM is used to support tag identification, data writing and reading. The core size of the analog front-end is only $0.94 \times 0.84\ mm^2$ with a power consumption of 0.42 mW. Measured results show that the power management circuit is able to maintain a proper working condition with an input antenna voltage range of 5.82–12.3 V; the maximum voltage conversion ratio of the rectifier reaches 65.92% when the tag antenna voltage is 9.42 V. Moreover, the power consumption of the 10% ASK demodulator is only 690.25 nW.

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1. Introduction

Radio frequency identification (RFID) is a technology which is widely used in many applications today, including supply chain management, personal identification, theft detection, air and train package and intelligent transportation [1,2]. Compared with other frequency band systems, applications of HF-band passive system are most widely used. For tags' designers, low power consumption and small size design is the developing trend of today's RFID tag chips, since power consumption decides the tag chip sensitivity (higher sensitivity means longer detection distance of the tag chip) while size determines manufacturing costs.

At present, the international standard protocols for 13.56 MHz RFID system are ISO/IEC 14443, ISO/IEC 15693 and ISO/IEC 18000-3. ISO/IEC 18000-3 protocol is recently proposed for item management. Besides, ISO/IEC 18000-3 provides physical layer, collision management system and protocol values for RFID systems for item identification operating at 13.56 MHz [3]. This new protocol has a relatively greater compatibility and can support more tags operating simultaneously.

In this paper, an analog front-end circuit of a 13.56 MHz passive RFID tag complying with ISO/IEC 18000-3 protocol is designed and fabricated. This paper mainly presents detailed design considerations of the proposed power management circuit and 10% ASK demodulation circuit. Specifically, this paper is organized as follows. Section 2 describes the RF link of the HF-band system and the system architecture of the proposed analog front-end. Section 3 presents the design of the power management circuit in detail. Section 4 presents the analysis and design of the proposed ASK demodulators. Measurement results are shown in Section 5. Finally, conclusions are drawn in Section 6.

2. RF link and system architecture

Unlike active tags which are energized by battery, the passive HF-band RFID tags are energized by a time-varying electromagnetic RF wave which is transmitted from the reader. HF-band system adopts inductive coupling to collect power, clock and data. Fig. 1 shows the inductive coupling model between the reader and tag. The tag antenna inductor L_{tag} and an off-chip capacitor C_{tag} form the RF tank circuit with the resonant frequency f (13.56 MHz). The mutual

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inductance M between the reader and tag is

$$M = \frac{k}{\sqrt{L_{reader} L_{tag}}} \tag{1}$$

where k is the coupling factor, which can be calculated by

$$k(D) \approx \frac{r_{reader}^2 r_{tag}^2}{\sqrt{r_{reader} r_{tag}} \left(\sqrt{D^2 + r_{reader}^2}\right)^3} \tag{2}$$

where r_{reader} and r_{tag} are the radii of the reader and tag antennas, respectively, and D is the distance between the reader and tag antennas [4].

Based on the principle of electromagnetic induction, the voltage amplitude V_{amp} of the tag antenna is

$$V_{amp} = N\frac{d\psi}{dt} = N\frac{d(\int B dS)}{dt} = 2\pi f NQAB \cos\alpha \tag{3}$$

$$B = \mu H \tag{4}$$

$$f = \frac{1}{2\pi\sqrt{L_{tag} C_{tag}}} \tag{5}$$

$$Q = \frac{R_{load}\sqrt{L_{tag}/C_{tag}}}{R_{tag} R_{load} + R_{tag}^2 + L_{tag}/C_{tag}} \tag{6}$$

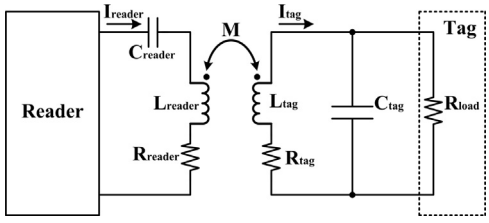

Fig. 1. Inductive coupling model between the reader and tag.

$$V_{amp} = 2\pi f NQA\mu H \cos\alpha = 2\pi f NA\mu H \cos\alpha \frac{R_{load}\sqrt{L_{tag}/C_{tag}}}{R_{tag} R_{load} + R_{tag}^2 + L_{tag}/C_{tag}} \tag{7}$$

where N is the turns of the tag antenna, f is 13.56 MHz, Q is the quality factor of the resonant circuit, A is the area of the tag antenna, B is the magnetic induction, α is the angle between the reader and tag antennas, H is the magnetic field intensity, μ is the permeability, and R_{load} is the equivalent load resistance of the tag chip.

According to test methods (ISO/IEC DTR 18047-3) for ISO/IEC 18000-3 protocol, A is 77 × 47 mm^2, N is 4. H is between 150 mA/m (rms) and 5 A/m (rms). When the angle α is 0, the voltage amplitude range of the tag antenna is

$$0.33Q \le V_{amp} \le 10.95Q \tag{8}$$

At 13.56 MHz the nominal inductance L_{tag} is 3.5 μH and the nominal resistance R_{tag} is 1 Ω [5]. From Eq. (6), the quality factor Q is mainly decided by C_{tag} and R_{load}. However, the voltage amplitude range of the tag antenna obtained from Eq. (8) is based on an ideal model. In fact, the energy propagation loss in the air, the distance between the reader and tag and other factors can further reduce the voltage amplitude V_{amp}.

Fig. 2 shows the block diagram of the proposed RFID transponder. The system is mainly composed of three sections, named antenna and resonant circuit, analog front end and digital signal processing unit. Antenna1 and Antenna2 are two ports connected to the tag antenna coil. The antenna (inductor L_{tag}) and the capacitor C_{tag} are external components to form the resonant circuit in order to ensure that the tag chip can obtain sufficient power supply.

The analog front-end is the key section to determine the performance of the whole tag chip. The rectifier converts the incoming RF power gained from the reader to a DC voltage. A storage capacitor C1 exists to store and supply power for the whole chip when the tag chip receives 100% ASK RF signal. A bandgap reference and two regulators form the voltage generator, thus generating precise and stable V_{CC} for analog front-end power supply and V_{DD} for digital unit power supply respectively.

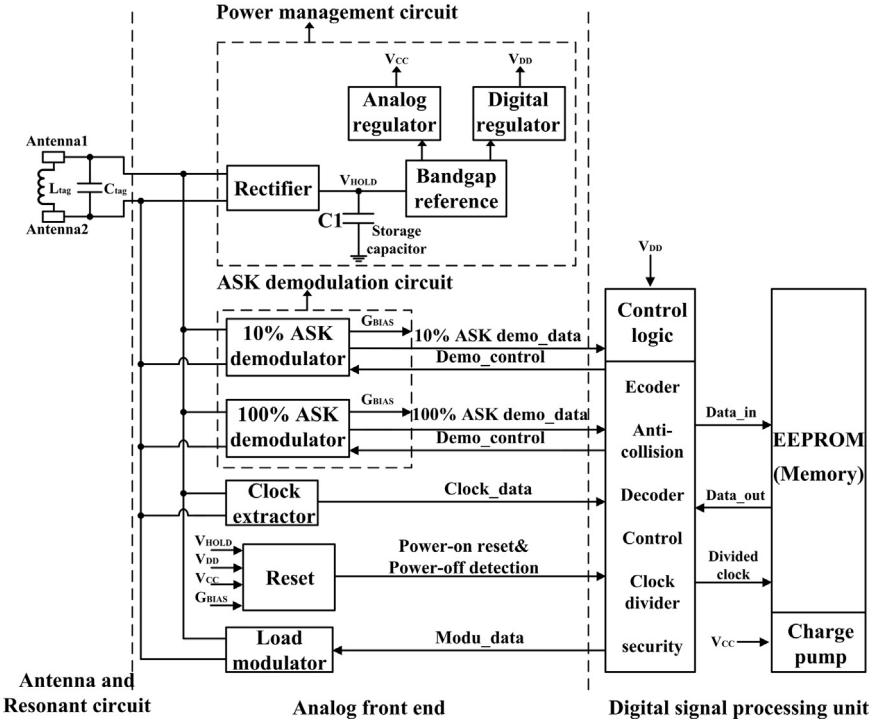

Fig. 2. Block diagram of the proposed RFID transponder.

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