Microelectronics Journal 45 (2014) 619–626

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A low power Ku phase locked oscillator in low cost 130 nm CMOS technology

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ARTICLE INFO

Article history:
Received 24 June 2013
Received in revised form
31 March 2014
Accepted 8 April 2014
Available online 4 May 2014

Keywords:
Ku band
CMOS
DVB-S
PLO
Microwave radiometer

ABSTRACT

This paper reports on a Ku low-power integer-N phase locked oscillator designed to investigate the potentialities of a low-cost 130 nm CMOS technology for video broadcasting and radiometry applications. The design and the characterization of the prototype are described and the main performances are reported and compared to literature. The PLO generates an output tone in the 14.2 GHz–15.1 GHz frequency range. The phase noise is −68.9 dBc/Hz for an offset frequency of 100 kHz from a 15 GHz carrier, and can be enhanced of about 20 dB. The circuit core sinks 23.7 mA from 1.2 V supply.

1. Introduction

Several mass market applications, as for example, Standard and High Definition TeleVision (SDTV and HDTV), interactive multimedia, data content distribution and professional TV applications use a portion of Ku band spectrum reserved for point to point and broadcasting satellite communications. Nowadays, in satellite receivers, the signal is picked up by the dish antenna and then amplified and down-converted by a low noise front-end. This block is frequently built using discrete compound semiconductor High Electron Mobility Transistors (HEMT) and Dielectric Resonator Oscillators (DRO), as well. This discrete approach is expensive due to components, assembling operations, and the resonator manual tuning [1]. A silicon-based monolithic integrated receiver offers advantages in terms of cost and size, specially when an integrated oscillator is used to replace the DRO. Nevertheless, performance limitations of integrated solutions are still restricting this kind of solution for penetrating high frequency mass market applications such as Digital Video Broadcasting Satellite (DVB-S) [2]. Some efforts have led to several prototypes as a monolithic 0.8 μm bipolar technology Low Noise Block (LNB) by STMicroelectronics [1], and more recently, a 0.25 μm SiGe:C commercially available BiCMOS technology LNB reported by NXP Semiconductors [2]. Avoiding the use of bipolar transistors is of great interest as well, which is the aim of [3,4], where a 0.18 μm CMOS LNA/down-conversion mixer chain and a LNB, respectively are claims. In all reported examples, the frequency synthesizer used to generate the local oscillator (LO) signal is a Phase Locked Loop (PLL). This kind of implementation requires a programmable frequency divider in the feedback loop. To easier demonstrate the potentiality of a technology for a given application where a local clock and/or a local frequency are required, the use of a Phase Locked Oscillator (PLO) is a good alternative because the frequency divider in a PLO exhibits a fixed modulus, making in this way easier its design. The present paper reports on the design and the characterization of a Ku-band PLO realized with a bulk 130 nm CMOS technology. The operation frequency was chosen so that to test its potentiality for both up-link (12.9–18.4 GHz) and down-link (10.7–12.75 GHz) frequency band. Particular attention has been paid on the phase noise which is the hardest specification to be satisfied. The modulations scheme (APSK) adopted in DVB-S standard exhibits indeed a round constellation where excessive rotational errors due to excessive phase noise would produce a burst of error [5]. The PLO can be also used as a local oscillator in the architecture of a microwave radiometric front-end [6]. Several applications in the microwave radiometry field, such as industrial harsh plants, where conventional sensors cannot be employed, or automotive safety, require cost and size reductions of the radiometer. For example, in order to keep low the cost, the emitted black-body radiation is usually detected with a

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http://dx.doi.org/10.1016/j.mejo.2014.04.013
0026-2692/

low cost printed antenna array [6,7], which size depends on the operation frequency. A PLO working at higher frequency allows therefore a reduction in the antenna size. For a 8×8 array patch-antenna with a gain of 25 dB, when the operation frequency moves from X-band to Ku-band, as in the present case, the antenna area shrinks of 2.5 times, from $10 \times 10\ \text{inch}^2$ to $6.3 \times 6.3\ \text{inch}^2$ [8]. Microwave radiometry is considered also an interesting solution for wild fire detection. In order to minimize the maintenance cost of the batteries, the microwave radiometer collocated in each node of the smart sensor network distributed on the wild area should be energy independent as much as possible, exploiting renewable energy sources, as integrated microphotovoltaic cells or harvesting circuits [9]. Dissipated power reduction is therefore a further parameter of paramount importance. Using, as in this case, low power technology allows to solve this constraint, making easier to target the energy independence of each node of the smart sensor network. When bias voltage moves from a 3.3 V of a 0.35 μm technology to a 1.2 V of a 130 nm technology, a significant reduction of the dissipated power has to be expected. Therefore, the use of a higher operation frequency and more scaled technology with respect to those reported in [6] allows to address the above discussed advantages of reduction in size and dissipated power. The present paper is organized as follows. Section 2 gives brief description of the used technology. The PLO architecture and the design of each building block are described in Sections 3 and 4, respectively. Experimental results are summarized in Section 5 followed by some considerations in Section 6. Finally conclusions are drawn in Section 7.

2. IC technology

The circuit is designed to fit with the commercial HCMOS9GP technology from STMicroelectronics. It is a triple well bulk CMOS technology with multiple voltage threshold transistors, for low leakage or high speed purposes, featuring an effective gate length of 130 nm. As shown in Fig. 1, the back-end features six copper layers with low-k inter-level dielectric and one aluminium layer on top [10–12]. The bias supply is typically 1.2 V even if the 2.5 V option is also available [11]. For the present design, low leakage, low threshold voltage transistors have been used with a supply voltage of 1.2 V. Several kinds of resistors are also available, as diffusion, salicied or unsalicied poly, and high resistivity poly resistors [13]. MIM capacitors, spiral inductors, and varactors are also available.

3. PLO architecture

Fig. 2 depicts the building block diagram of the designed PLO. It is constituted by a Phase Frequency Detector (PFD), a Charge Pump

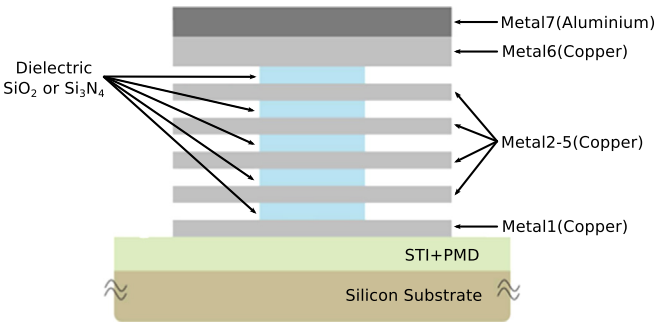

Fig. 1. 130 nm CMOS STM technology (HCMOS9GP).

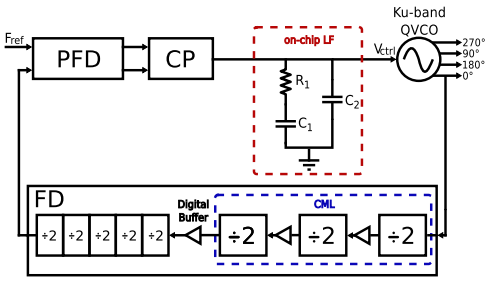

Fig. 2. Phase locked oscillator blocks diagram.

(CP), a second order Loop Filter (LF), a Frequency Divider (FD), and a Quadrature Voltage Controlled Oscillator (QVCO). The difference with respect to an N-integer PLL is that the FD in the PLO exhibits a fixed modulus while in the PLL the FD is constituted by two blocks: the prescaler, a dual-modulus frequency divider guaranteeing a frequency resolution equal to the reference frequency, and a programmable section, usually implemented with down counters. It is worth here reminding that the design of the VCO/FD interface is the challenging step in the design flow of the loop, specially when the first block of the FD is the pre-scaler. The PLO architecture with its fixed modulus FD offers therefore the advantage of making a bit less critical the design of this interface. Once the potentiality of the addressed technology for a given application is demonstrated, efforts can be spent to design a programmable FD, to obtain a PLL from the PLO, in the case a PLL would be required. The frequency division ratio (256) of the FD is set for enabling the generation of a Ku-band tone from an external reference frequency f_{ref} of about 60 MHz. The frequency divider is implemented as eight division-by-two stages. The first three stages are designed using a Current Mode Logic (CML) to achieve high operation frequency. Each CML stage is buffered in order to be able to drive the following divider stage. The division chain is completed with five low power digital frequency dividers realized with transmission gate registers. Because of the QVCO implementation, four output phases are available at PLO outputs. Finally, it is worth noticing that the loop filter is integrated on die for low cost considerations.

4. PLO design

4.1. Quadrature VCO

For generating signals in quadrature, the main techniques usually used are poly-phase filters, ring oscillators or frequency dividers. Nevertheless, in the present work two cross-connected symmetric LC VCOs have been preferred, because of their good phase noise performances.

The schematic of the QVCO is depicted in Fig. 3 and was previously reported in [14]. Here some features and performances are quickly reminded; more details are available in [14]. The circuit is biased without current mirror to minimize the phase noise, the power consumption, and also to avoid any automatic control circuit. All transistors exhibit the minimum gate length. The width of PMOS transistors must be wide enough to ensure robustness against fabrication tolerances. The octagonal inductor in the tank exhibits an inductance of about 290 pH and a maximum quality factor of 27. The tuning capability is achieved using two 20 fingers MOS varactors with a minimum gate length of 350 nm. For a carrier frequency ($f_{carrier}$) of 15 GHz, the dissipated power (P_{DC}) is 11 mW and the measured phase noise L(Δf) is -106 dBc/Hz for a carrier frequency offset (Δf) of 1 MHz.