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A SiGe LC-ladder low noise amplifier with base resistance match, gain and noise flatness for UWB applications

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ABSTRACT

This study presents a 3.1–10.6 GHz ultra-wideband low noise amplifier (UWB LNA) in 0.18 μm SiGe HBT technology. To achieve a good input match, parasitic base resistance in a bipolar transistor and an LC-ladder filter are included into calculations with the common-emitter topology using shunt–shunt capacitive feedback. Both high and flat power gain (S_{21}) and low and flat noise figure (NF) are achieved by adjusting the pole and zero in amplifying stage and quality factors of the fourth-order input network. Design equations for performances such as gain, noise figure and linearity IIP3 are derived especially on gain flatness and noise flatness. LNA dissipates 33 mW power and achieves S_{21} of 20.65+0.7 dB, NF of 2.79+0.2 dB over the band of 3.1–10.6 GHz. The simulated input third-order intermodulation point (IIP3) is −17 dBm at 10 GHz.

1. Introduction

With the approved application of ultra-wideband (UWB) technology for commercial use in early 2002, ranging from 3.1 to 10.6 GHz, the availability of such high bandwidth allows higher data throughput up to 500 Mb/s. Besides, flat and low NF frequency response is required [1–5]. Conflicts exist between flat gain and flat NF responses [6,7], so optimization of wideband noise flatness in addition to a flat gain response is required. Noise usually deteriorates at high frequency due to the circuit-performance degradation caused by the high sensitiveness to capacitance and inductance. Therefore, the factors governing the shape of NF at high frequency should be identified and modified.

Two methods are usually adopted in the noise optimization; one is to use a resistor capacitor (RC) network or resistor inductor (RL) terminal network with a specific terminal resistance to replace the traditional 50 Ω terminal resistance for the gate transmission line [3,5]. This can reduce the noise contribution at the expense of a little degradation in the input matching. However, this technique usually requires a large area which means that a distributed amplifier (DA) usually adopts this method. The first method is not cost efficient and the second method is to use the intrinsic attribute to achieve the input match and flat noise. Chen et al. [6,7] have introduced a RLC branch at the input of LNA and tuned the under-damped Q network to achieve a good input match and noise flatness simultaneously. This approach can save the die area because no extra devices are required to achieve the flat noise; besides, extra components may itself introduce an undesired noise contribution. Both methods use the under-damped Q network to optimize the noise performance; however, some differences are obvious: the first one is to adjust the input impedance along with the frequency; this can directly change the weight and the source noise contribution at different frequencies. The second one does not change the source contribution too much; the influences which affect the noise shape at high frequency are identified the most and by adjusting the input second-order network, the shape is trimmed to a flat one.

With the convenient and cost-efficient quality, this paper adopts the second method to implement a LC ladder two-stage LNA. Compared to the research in Ref. [6], this paper introduces a fourth-order network to optimize the noise figure. Even though this schematic is almost the same as what professor Abidi has declared in Ref. [13] except some changes in the second stage for gain flatness, noise flattening was not optimized at that moment, more noise optimization can be achieved due to the merit of LC structure. High order network means difficult analysis, so in order to address this problem detailed derivations are executed to fulfill the noise trimming. Base parasitic resistance is first considered in the analysis of input match. Gains in two stages are allocated at two different center frequencies to achieve gain flatness as well as avoid one-stage gain overshoot which results in non-linearity. A shunt–shunt feedback topology at input terminal is used to realize good S_{11} and ensure comparable low noise; and loading inductor in the second stage is used to decrease the difficulties in input matching and enhance high frequency gain of LNA.

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This paper is organized as follows: Section 2 discusses CMOS and bipolar input match schemes, the source/emitter degeneration type and shunt–shunt feedback topology, and modifications on SiGe technologies are discussed in detail. Section 3 introduces the design of proposed LNA including input match, gain flattening, noise flatness optimization and linearity consideration. Section 4 discusses the experimental results, which is followed by conclusion in Section 5 and acknowledgment.

2. Discussions on input match topologies

2.1. CMOS input match topologies

There are several methods to implement the wideband input match in LNA, and the main theory in input match is to maintain the input impedance to look like a real resistance, 50 Ω. Low Q filter networks are gladly used [6,8,9] with the fact that their bandwidth at resonance is large compared to that of the high Q network. Two topologies are mostly used: the source degeneration type and shunt–shunt feedback type. Inductive source degeneration LNA is firstly used in narrow band LNAs [10–12] because of the easy design and implementation, as well as good noise. Shunt–shunt feedback topology is better than common gate structure whose drain current noise increases a lot at high frequencies, but feedback scheme can suppress the noise to a satisfying amount [13–17]. Besides, multi-order filters in feedback network can ensure a wide input match.

Fig. 1 shows two input topologies: (a) and (b). G_M is the effective transconductance of transistor and Z_{LOAD} is the load impedance, R_L is the real part of Z_{LOAD}. The equivalent real part R_{IN} of Z_{IN} is a bit complicated, indicated as

$$R_{IN} = \frac{R_L}{(1+G_M R_L)}[(C_F + C_{GD})/(C_{GS} + C_F + C_{GD})]^2 \approx 50\ \Omega \quad (1)$$

Both topologies can ensure a wide band input match. Attention should be made that C_F exists in the small-signal circuit of (b) topology whereas does not in (a); actually C_{GD} in (a) also affects the match performance. Miller capacitor C_{GD} will couple the load effect into the gate of transistor, leading to a more complex impedance which is hard to tune. Moreover, in order to achieve a high gain large-size transistors are preferred; this will simultaneously increase the Miller Effect; high frequency gain will drop more drastically and noise performance may deteriorate at high frequency band.

The other concern is of loading effects. Z_{LOAD} usually consists of a resistor and a capacitor which is mainly contributed by the next amplifying stage. With Miller's coupling, the input impedance contributed by the load is a complex value which deteriorates the input match. Inductor load can ensure a high gain, but is not preferably used. This is because loading inductor and parasitic capacitor will introduce a second-order network which can easily make the input tuning and is very hard to implement. Fortunately, several methods can alleviate this problem; one is to change the position of the inductor at second or third stage, enhancing the intrinsic isolation between the inductor and input terminal. The other way is to use a cascode topology; this will decrease the Miller Effect and loading effect, only at the cost of high voltage supply and more power dissipation.

2.2. Modification on two bipolar topologies

Corresponding to CMOS input topologies there are some modifications on these two schemes. The most significant differences result in the device structure and the base resistance, as shown in Fig. 2.

Base resistances should be considered in these structures. The impact in (a) can be tuned in a manner that the input resistance is the sum of base resistance r_{bb} plus inductor-introduced resistance $\omega_T L_S$. This is easy to implement only with the caution that makes $\omega_T L_S$ less than 50 Ω. r_{bb} may degrade the gain of LNA, but with increasing load ; this small degradation amount can be omitted. The small-signal circuit in (b) is an intermediate topology, separating the loading impedance as a branch of RC series. In (b), however, the base resistance's effect worsens the input match. That is because the transformation from two branches into one RLC series is based on the assumption that C_{BE} is a pure capacitor, not with a series resistance [8].

Fig. 3 shows a Smith Chart of small-signal input match in Fig. 3(b) with and without r_{bb}, ranging from 2 to 16 GHz. As can be seen, even though base parasitic resistance is not a large amount,

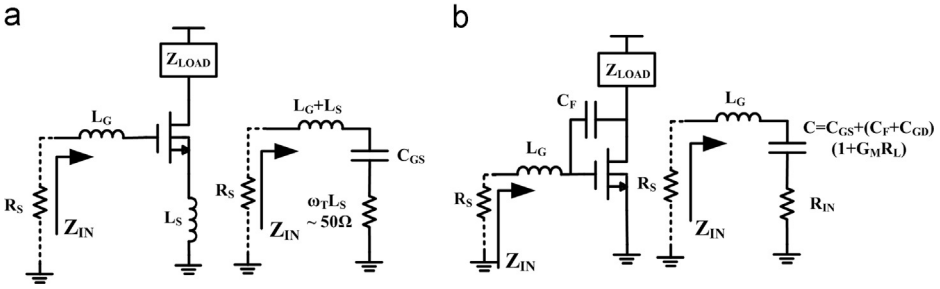

Fig. 1. Schematic and small-signal circuits of two input match techniques: (a) inductive source degeneration; (b) shunt–shunt feedback.

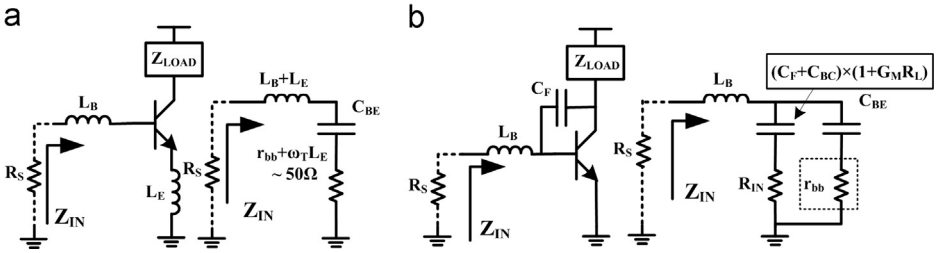

Fig. 2. Schematic and small-signal circuits of two input match techniques: (a) inductive emitter degeneration; (b) shunt–shunt feedback.