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A fully integrated feedback AGC loop for ZigBee (IEEE 802.15.4) RF transceiver applications

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ABSTRACT

This work presents an efficient solution for automatic gain control (AGC) loop in ZigBee transceiver compatible to IEEE 802.15.4 standard. The design is based on a RF (Radio Frequency) and linear IF (Intermediate Frequency) chain where the signal amplification is done in the RF front-end blocks and analog VGAs (variable gain amplifiers). The gains of the RF block and VGA are digitally controlled by the DAGC (Digital AGC) block to ensure that the ADC (Analog-to-Digital Converter) operates inside its dynamic range. Feedback loop architecture is employed for the advantage of high linearity due to its inherent characteristic. The whole AGC loop has been integrated in the ZigBee transceiver which was fabricated in a 0.18 μm CMOS technology. The AGC loop achieves a dynamic range of about 95 dB with the gain error of less than ± 0.5 dB. The two-channel VGAs and peak detectors occupy an area of 1.5 mm × 0.4 mm and dissipate 1.71 mW from a single 1.8 V power supply. The DAGC has been integrated in the digital baseband processor and occupies an area of about 0.4 mm × 0.4 mm. The max gain lock time of the AGC loop is about 1.25 μs.

1. Introduction

In most wireless communication transceiver applications, the power of the received signals is rarely constant due to many factors such as environments, distances, weather, terrains and so on [1]. Traditional ADCs do not have large enough input dynamic range to accommodate these strength variations of the signal. Therefore, it is advantageous to design the signal processing chain with ability of continuously adapting its gain to the signal amplitude [2–4]. One of the most popular solutions is to utilize AGC loop which inserts a large dynamic range and high linearity VGA block in front of the ADC and adjusts the VGA with digital control words [5–8]. Peak detectors or power estimators are usually employed to obtain the information of the signal strength and on which the DAGC block is based to generate digital control words. A typical feedback AGC loop scheme consisted of a variable gain amplifier, a power detector, a loop-filter (LPF) and the digital AGC block is shown in Fig. 1. The gain control circuitry—DAGC block must be accurately designed to implement a linear-in-dB control characteristic. The dynamic range and gain resolution of the whole loop is mainly determined by the VGA [9].

ZigBee transceiver features low-rate, low-power and low-cost. Combination circuits such as VGLNA (Variable Gain Low Noise Amplifier) which combines LNA and VGA, VGM (Variable Gain Mixer) which combines Mixer and VGA have been developed for low power consumption in the previous published works [3,10–13]. If the RF blocks achieves a 20–30 dB dynamic range, the design of the analog baseband VGA can be relaxed and much lower power consumption can be realized. According to IEEE 802.15.4 standard, the ZigBee receiver chain should achieve a dynamic range of about 95 dB assuming a 10 dB margin to meet the −85 dBm sensitivity requirement [14]. Given 0–25 dB gain provided by the RF block including LNA and Mixer, 70 dB dynamic range should be achieved by the VGA.

In this paper, the proposed AGC loop and gain adjustment mechanism for ZigBee transceiver applications are presented. Section 2 details the system configuration of the AGC feedback loop and the analog VGA scheme. Section 3 describes the adjustment mechanism of DAGC block. The experimental results are given in Sections 4 and 5 is the conclusion.

2. AGC loop architecture

The architecture of the proposed AGC loop inside a low intermediate frequency (Low-IF) ZigBee receiver is shown in Fig. 2. The RF block is designed to be programmable and can be set to three different gain levels—high (30 dB), medium (14 dB) and low (−2 dB). Two digital control bits noted R[1:0] are

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generated by the DAGC to determine which level should be adopted. Peak detectors play an important role in this loop that they link the analog circuits and the digital control block, extract the amplitude of VGA outputs and compare the outputs with the reference voltage V_{ref} [15]. Then, a 5-bit comparison result is fed into the DAGC block after being filtered by a capacitor and the DAGC outputs S[4:1], T[2:0] and R[1:0] to set the gains of VGA and RF front-end blocks respectively.

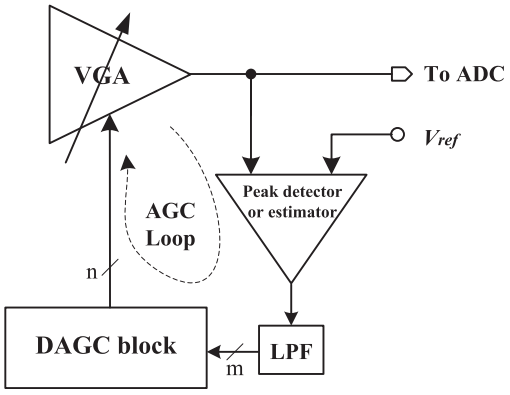

Fig. 1. Architecture of a typical feedback AGC loop.

The VGA used in this paper consists of two stages named respectively coarse tuning stage and fine tuning stage as shown Fig. 3. Fully differential scheme is adopted to ensure a better common mode noise rejection. The coarse tuning stage achieves 56 dB dynamic range with a 4-bit control signal S[4:1]. Switches are controlled by the combinations of S[4]∼S[1] and if the value of the combinational logic expression is "1", e.g. S[1]S[2] is "1" when S [1] is "1" and S[2] "1", the switches controlled by this logic will be tuned on while "0" turned off. Meanwhile, each bit in S[4:1] corresponds to one sub-stage, i.e. if S[1] is "1", stage1 will be active while "0" bypassed.

Each of the sub-stages in the coarse tuning stage employs a common source (CS) differential amplifier with resistive loads (R_L) as shown in Fig. 4 to meet the 14 dB gain requirement. A unit gain buffer is used to provide common mode voltage for the input differential pairs M1 and M2. Input signals V_{inp} and V_{inn} are ac coupled to M1 and M2 by capacitor C and pulled up to V_{ref} by a resistor R_p. Source resistive feedback (R_f) is employed to enhance the linearity of the amplifier. The gain can be easily caculated as $A_v \approx -R_L/R_f$. The fine tuning stage is implemented as shown in Fig. 5 by an operational transconductance amplifier(OTA) and

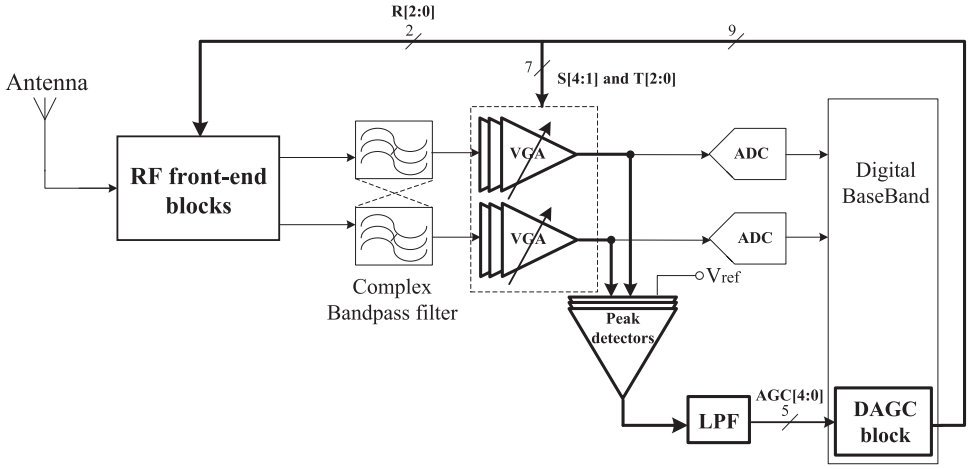

Fig. 2. Block diagram of proposed AGC loop inside the ZigBee receiver.

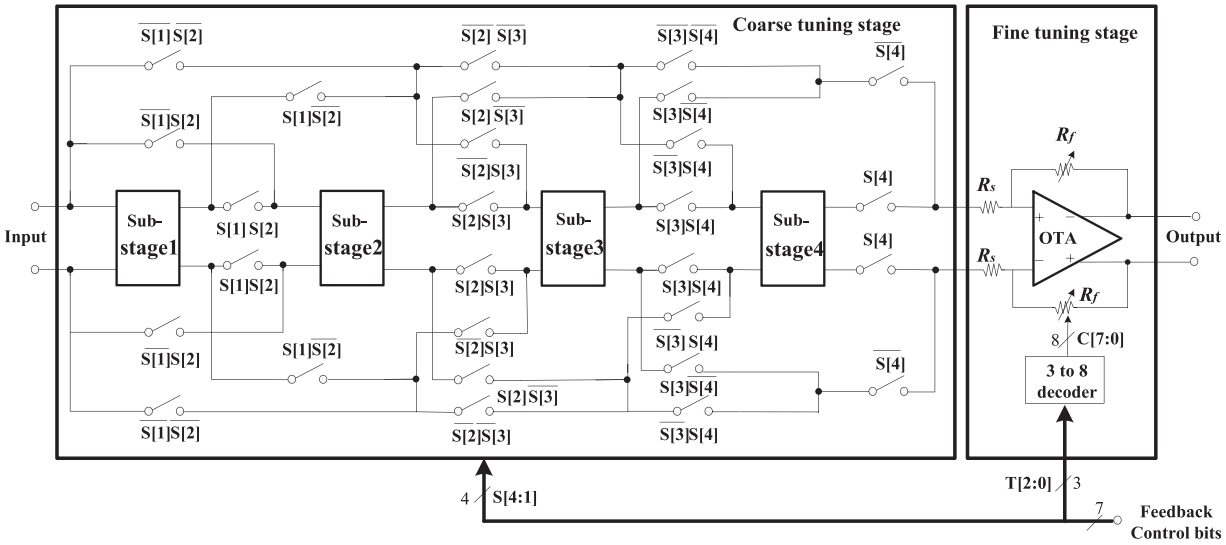

Fig. 3. VGA structure employed in this work.