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Review

Atomic layer deposition of high-k dielectrics on III–V semiconductor surfaces

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Abstract

The goal of this article is to provide an overview of the state of knowledge regarding the Atomic Layer Deposition (ALD) of metal oxides on III–V semiconductor surfaces. An introduction to ALD, the band structure, various defects present on the III–V surface and how they relate to Fermi level pinning are discussed. Surface passivation approaches are examined in detail in conjunction with experimental and computational results. The "interface clean-up" reaction that leads to the formation of a sharp gate oxide/semiconductor interface is related to the surface chemistry and the transport of the surface oxides through the growing dielectric film. Finally, the deposition of metal oxides on semiconductors is discussed in the context of interface quality and some examples of devices using III–V channels and ALD metal oxides are given.

Keywords: Atomic Layer Deposition; Dielectrics; III-V semiconductors; Interface clean-up; Fermi level pinning

1. Introduction

Atomic layer deposition is a very powerful technique for the deposition of coatings with very high level of thickness and composition control. It is based on self-limiting chemical reactions and as a result can coat with a very uniform layer not only planar surfaces but also very high aspect ratio features. Developed originally as atomic layer epitaxy by Suntola, its popularity and applications have exploded in the past fifteen years [1]. The semiconductor industry at the same time has been pushing the boundary of the design parameters for the metal oxide semiconductor field effect transistors (MOSFET), which are the building blocks of the integrated circuit (IC). Several physical limits have been reached for the traditional materials forcing the introduction of novel materials such as high-k dielectrics and metal gates [2–8].

As the nano electronic industry started introducing new gate oxides and gate metals the longtime attachment to the Si channel stemming from the high quality Si/SiO_2 interface was challenged and the industry has been looking for other channel materials that will allow the full exploitation of the properties of the new materials. Higher mobility substrates, such as Ge and III–V semiconductors, have been well known for decades and have better inherent electrical properties than Si, but one major obstacle in their utilization for complementary metal oxide semiconductor (CMOS) devices has been the absence of a high quality native oxide [4]. However, the extensive study of high-k dielectrics in the past twenty years has provided several other insulating materials that can be used in lieu of SiO_2. The emergence of ALD as a technique that allows the deposition of such dielectric with high thickness precision and composition control has provided an additional incentive to take an extended look to substrates such as III–V semiconductors. One of the most noteworthy observations for III–V/high-k dielectric gate stacks has been the ability to obtain a

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sharp interface between the substrate and the gate dielectric. This is in stark contrast to Si/high-k gate stacks that with the exception of Al_2O_3 a sharp interface is elusive creating a host of other issues [9–12]. Apart from the absence of a high quality native oxide the most common problem associated with III–V gate stacks is the so-called "Fermi level pinning" which is attributed to a significant density of interface defect states [13–15]. However, since surface passivation approaches have been found to reduce the density of the interface defects there is every expectation that well behaved ICs utilizing the full potential of the dielectric and the channel material can reach the commercial electronics market in the foreseeable future.

The goal of this article is to provide an overview of the state of knowledge regarding the ALD of metal oxides on III–V surfaces focusing mainly on interface structure and quality issues. The consumption of the surface native oxides during the ALD of dielectrics on III–V surfaces, the so-called "interface clean-up" reaction, is discussed and an overview of the recent development in the understanding of the surface chemistry is given. Finally, a brief outlook for the III–V based devices is given.

2. Atomic layer deposition

Atomic layer deposition is a thin film deposition technique that allows atomic level control of the process, and achieves very smooth, uniform, conformal films even on very high aspect ratio structures [16]. In the ALD process film formation is achieved by alternating exposure of a surface to the vapor of two chemicals that react in a complementary, self-limiting manner [17]. Complementary means that each of the two reagents prepares the surface for reaction with the other chemical so the process is cyclical. Reactions are self-limiting if the amount of material deposited per exposure is uniform over the surface, assuming that a saturating dose of precursor reaches each part of the surface. Both the precursor adsorption and the exchange reaction between the chemisorbed surface species and the second reagent are thermally activated processes, and usually the energy is provided by heating either the substrate or the entire chamber. A typical atomic layer deposition process consists of four steps (Fig. 1):

i. a self-terminating reaction of a suitable precursor (reactant A) on a functionalized surface to produce a chemisorbed species submonolayer and possibly volatile products;
ii. evacuation or purging of the precursors and any by-products from the chamber;

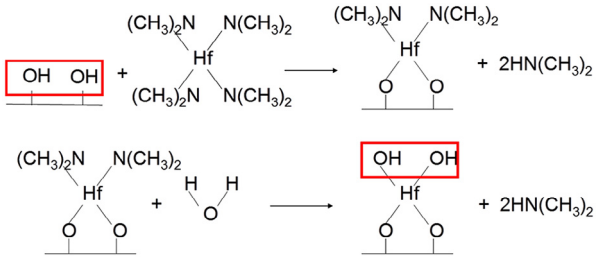

Fig. 1. A cartoon that depicts the reaction sequence for the formation of HfO_2 films using tetrakis dimethyl amino hafnium and H_2O. Note the cyclic nature of the process as well as the presence of OH surface termination.

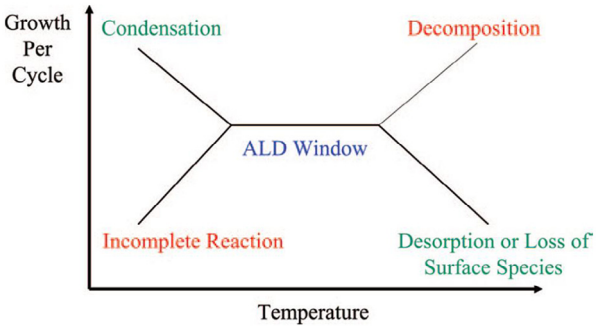

Fig. 2. Typical trends of growth rate per cycle (GPC) as a function of temperature for an ALD process. Most well behaved ALD processes operate in the flat region called ALD window [18]. Reproduced with permission from the American Chemical Society.

iii. a self-terminating reaction of the other reactant species (reactant B) or another treatment to activate the surface for reactant A;
iv. evacuation or purging of the reactants and by-product molecules from the chamber. At this point the surface has returned to its original condition and the cycle can be repeated.

Strictly speaking there is a fairly narrow temperature window for a thermal ALD process (Fig. 2) [17,19]. At low temperatures incomplete/slow chemisorption of the precursor or limited reaction may result in incomplete stripping of precursor ligands. At higher temperatures precursor decomposition may result in increased carbon incorporation in the film similar to a typical CVD process. Although the majority of ALD processes developed are based solely on thermal activation, plasma enhancement has been used to provide a means to achieve film bonding and stoichiometry not accessible through thermal processes [20,21]. Interest in ALD has increased substantially in the past decade due to the unique features and capabilities of the process such as linear