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Localization of temperature sensitive areas on analog circuits

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ABSTRACT

We introduce a novel easy to apply method to detect critical temperature sensitive areas on analog circuits. Our method is based on heat diffusion on a silicon micro-chip: the corners of a temperature sensitive micro-chip are heated up directly by ESD diodes or infrared laser light. This heat stimulus at the corners results in an inhomogeneous temperature distribution. Thus, the temperature is a function in time and space. The elapsed time to change the chip status from "fail" to "pass" as a reaction to the heat stimulus correlates with the distance to the heat source. This correlation is extracted from COMSOL simulations and experimental results. A numerical program based on that correlation succeeded in localization of the temperature sensitive chip module.

Micro-chips affected by corner MOSFETs in the subthreshold regime are used to demonstrate our method.

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1. Introduction

The correct operation of semiconductor micro-chips has to be ensured at various ambient temperatures. In semiconductor industries, therefore, the Circuit-Under-Test (CUT) is homogeneously heated up or cooled down while a complete test pattern is run. Chips which meet all required specifications in the test flow for tested temperatures are labeled as "pass", otherwise as "fail".

The temperature influences a wide spectrum of electrical and physical chip parameters [1,2]. Accordingly, the impact of local malfunctions on chip functionality may vary with temperature. The malfunctions may be enhanced when temperature is increased or decreased. Thermal Laser Stimulation (TLS) techniques are commonly used for directly localizing faults [3,4]. However, the TLS techniques face many challenges regarding chip preparation and fault localization [5–7].

Our proposed method uses heat diffusion for localization. It benefits from its simple set-up, which requires only standard test equipment. ESD diodes biased in the forward direction can be used as a heat source [8]. This avoids time-consuming chip preparation.

In the following, the method of heating the corners of a chip for localization of temperature sensitive corner devices is introduced. Further, the investigation of chips without errors in terms of temperature sensitive spots can be profitable. It may point to unknown critical circuits which demand high fabrication precision.

The paper is organized as follows.

Chapter 2 of this paper is focused on an understanding of temperature sensitive corner devices. The corner device in this context shall illustrate how parasitic effects may be affected by the variation of temperature.

Chapter 3 presents the localization methodology based on heat diffusion considerations.

Chapter 4 is dedicated to the experimental set-up and the localization results.

Finally, Chapter 5 discusses the chances and difficulties to transfer the proposed methodology to a wafer level test.

2. Temperature sensitive corner devices

2.1. Effects of temperature on devices

The most important electrical parameter in modeling MOSFETs is the threshold voltage V_{Tn} [9]. V_{Tn} represents the onset of drain–source current flow. For low gate–source voltage V_{GS}, V_{Tn} mainly controls the temperature dependency of the drain–source current I_{DS} [10]. Several existing methods to determine the threshold voltage are reviewed in [9]. Few of these threshold extracting methods consider the weak inversion region of a semiconductor [9]. Shifts in the onset of weak inversion due to parasitic effects, such as drain–source leakage currents, remain hidden. For transistors operating in

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the subthreshold regime (see 2.2) this situation is very unsatisfactory.

2.2. Subthreshold operation and corner device

When the gate–source voltage V_{GS} is below the threshold voltage V_{Tn}, the transistor operates in the subthreshold regime. In this state the semiconductor is in weak inversion and the drain–source current is dominated by diffusion of minority carriers in the channel [11,12]. The drain–source current has an exponential dependency on the gate–source voltage like a bipolar transistor and the current is very small (~nA). So, devices operating in the subthreshold region are ideal for ultra low power applications [12]. The corresponding drain–source current I_{DS} is given by

$$I_{DS} = \frac{W}{L}\mu_n^{300\ \mathrm{K}}\left(\frac{T}{300\ \mathrm{K}}\right)^{-1.5} C'_{ox} n \left(\frac{26\ \mathrm{mV}}{300\ \mathrm{K}}T\right)^2 \times \exp\left[\frac{1}{n}\frac{300\ \mathrm{K}}{26\ \mathrm{mV}}\frac{1}{T}(V_{GS}-V_{Tn})-1\right] \times \left(1-\exp\left[-\frac{300\ \mathrm{K}}{26\ \mathrm{mV}}\frac{1}{T}V_{DS}\right]\right) \quad (1)$$

for a gate–source voltage $V_{GS} < V_{Tn} + n(26\ \mathrm{mV}/300\ \mathrm{K})T$.

W/L is the channel dimension, $\mu_n^{300\ \mathrm{K}}$ is the electron mobility at 300 K, T is the temperature, C'_{ox} is the gate oxide capacitance per square, V_{DS} is the drain–source voltage and n is a dimensionless number in the range of 1.5–2.5 [10]. The second line in Eq. (1) indicates the exponential dependency of the drain–source current on V_{GS}.

Inherent to Shallow Trench Isolation (STI) technology is fringing gate fields that enhance carrier inversion within the silicon corner at the isolation edge. As a consequence, there is a low threshold voltage V_{Tn} path at the silicon corner that conducts in parallel with the MOSFET channel region [13]. This effect leads to a so-called "corner device" and is increased if gate metalization wraps around the channel edge.

2.3. Measured characteristics of a corner device

For transistors operating in the strong inversion regime the corner device effect can be neglected due to higher drain–source currents. In contrast, in the subthreshold regime the corner may strongly influence the $I_{DS} - V_{GS}$ characteristic. This is demonstrated in Fig. 1 for NFETs of equal designed length ($L = 1\ \mu$m) and equal designed widths ($W = 20\ \mu$m) affected by corner devices and not affected by corner devices. The logarithmic drain–source current $\log(I_{DS})$ and its derivative – which is the transconductance g_m divided by I_{DS} – is plotted versus gate–source voltage V_{GS} at a drain–source voltage V_{DS} of 2.5 V and a substrate voltage V_{BS} of -2 V. The lower threshold voltage path at the silicon corner results in higher leakage currents for the corner device affected NFET in the transistor "off" – state ($V_{GS} \le V_{Tn} \approx 0.8\ V$) remarkable in the logarithmic plot. The crossover in the derivative of $\log(I_{DS})$ ($V_{GS} = 0.5\ V$) is determined by the threshold shift to lower voltages for corner devices and by the transition from an increasing corner current to saturated corner current. The minimum in the derivative of $\log(I_{DS})$ marks the gate–source voltage V_{GS} where the channel starts to contribute a significant component to the total current.

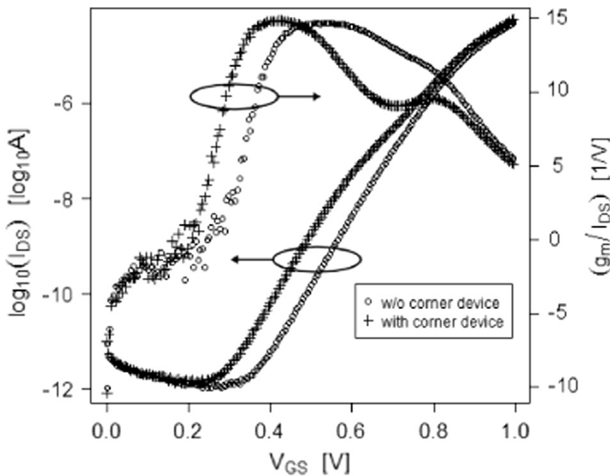

Fig. 1. Logarithmic $I_{DS} - V_{GS}$ characteristic and its derivative of $V_{DS} = 2.5$ V for a NFET (see text for details) affected by corner devices and a NFET not affected by corner devices.

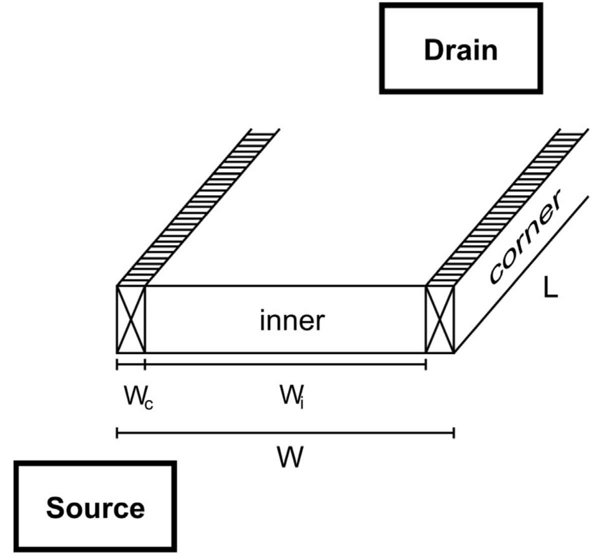

Fig. 2. Transistor model of a corner device with the inner channel width W_i and the corner channel width W_c and equal length L.

In the following, a transistor affected by corner devices is modeled as a "inner" transistor with two "corner" transistors in parallel. Both types are physically distinguishable only in their channel width (Fig. 2). The threshold voltage of the "corner" transistor is lower than that of the "inner" transistor.

The total current for a corner device $I_{DScd} := \hat{I}_{DS}$ in the subthreshold regime then becomes

$$\hat{I}_{DS} = \hat{I}_{DSi} + \hat{I}_{DSc} \quad (2)$$

where $\hat{I}_{DSi}$ is the contribution of the inner transistor to the total current and $\hat{I}_{DSc}$ is the contribution of the corner transistor to the total current. The currents $\hat{I}_{DSi}$ and $\hat{I}_{DSc}$ can be redefined in the following way:

$$\hat{I}_{DSi} := W_i \cdot i_{DSi} = W_i \cdot i_{DS},$$
$$\hat{I}_{DSc} := 2W_c \cdot i_{DSc},$$
$$W := W_i + 2W_c \quad (3)$$

where i_{DSi} and i_{DSc} are current layers along L for the inner device of width W_i and the corner device of width W_c, respectively. i_{DSi} is equal to the inner current layer in a transistor without corner devices. The sum of both widths gives the total width W. Eq. (2) can then be rewritten, giving

$$\hat{I}_{DS} = (W - 2W_c) \cdot i_{DS} + 2W_c \cdot i_{DSc} = W \cdot i_{DS}\left(\frac{W-2W_c}{W} + \frac{2W_c}{W}\frac{i_{DSc}}{i_{DS}}\right) \quad (4)$$

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