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A new tunable current-mode peak detector

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ABSTRACT

The paper presents a completely new realization of peak detector/full-wave rectifier of input sinusoidal signals employing four CCCIIs (controlled current conveyors), metal-oxide–semiconductor transistors and a single grounded capacitor, without any external resistors and components matching the requirements. The circuit gives a DC output voltage that is the peak input voltage over a wide frequency range, with a very low ripple voltage and low harmonic distortion. The proposed circuit uses an all-pass filter as a 90° phase shifter of the square value of the processed input signal. The proposed circuit is very appropriate to be further developed into integrated circuits. To verify the theoretical analysis, the circuit HSPICE simulations were also included, showing good agreement with the theory.

1. Introduction

Precise full-wave rectification function is one of the important requirements in many applications, such as instrumentation and measurement [1,2]. It is generally used in AC voltmeters and ampermeters, signal-polarity detectors, averaging circuits, sample-and-hold circuits, peak value detectors, clipper circuits, and amplitude-modulated signal detectors. In all of these applications, the use of a diode to provide the rectification has the serious drawback of having to overcome the threshold voltage of the diodes, which prevents the rectification of signals below a voltage of about 0.6 V. An operational amplifier (OA) with its high open-loop gain can be used to overcome the diode threshold voltage, thus permitting the rectification of low-level signals. This class of circuit generally performs well at low frequencies, however it produces moderate to severe waveform distortion at frequencies above about 1 kHz [3]. This is due to the fact that the diodes are OFF at the crossover point of the input signal, causing the OA to operate in an open-loop configuration. As the signal frequency increases, slew-rate limiting increasingly prevents the OA from turning ON the diodes rapidly, which causes distortion. It is possible to overcome this problem by using a second-generation current conveyor.

The current-mode (CM) circuits, such as the second-generation current conveyors CCIIs, have received considerable attention due to their better linearity, wider bandwidth, larger dynamic range, and low power dissipation compared with their voltage-mode counter-parts, such as operational amplifiers (OAs) [3–5]. The CCIIs, first introduced in [6], are functionally flexible and versatile. Thus, they have been used in a large number of different applications such as universal filters, inductor simulators, capacitance multipliers, oscillators, full-wave rectifiers [7–11], etc. High output impendence of the CCIIs enables overcoming the turn-on resistance of the diode and permits the rectification of low-level signals (in most cases rectifier was diode based), as well as responding to frequencies exceeding 100 kHz. However, the CCII cannot control the parasitic resistance at x (R_x) port therefore, when it is used in circuits, it inevitably requires additional external passive components, especially the resistors. This does not allow IC implementation as it requires large chip area, results in high power dissipation and defies electronic controllability. On the other hand, the introduced second-generation current controlled conveyor (CCCII) has the advantage of electronic adjustability over the CCII [12]. Also, the use of dual-output current-conveyors can be useful in the derivation of current-mode single input circuits.

In paper [8,10], the frequency range was extended by using voltage and current biasing schemes. While these circuits produce lower distortion and have a wider bandwidth than the OA-based class of circuits, the accuracy is inferior to that of the OA-based circuits. This occurs because of the imprecision of the transfer function, which involves the resistance at the inverting input of each current conveyor. The use of the current conveyor to improve performance of an OA-based circuit was discussed further in [13]. Full-wave rectifiers based on a CMOS class AB amplifier and current rectifier operation are described in [14,15]. This circuit offers a wide dynamic range and shows a broadband operation. CMOS integrated active rectifier concept is an innovative approach for higher efficiencies [16]. These rectifiers provide output voltages nearly at the level of the input voltage combined with low power

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consumption, which was also achieved through the circuit design proposed here. In [17], a single CCCII-based precision full-wave rectifier circuit is proposed using a three-output CCCII, two MOS transistors and a resistor with large cross-over distortion for a low frequency of 5KHz. In [18,19], full-wave rectifier circuits are proposed using two second-generation current conveyors (CCIIs) and four diodes.

The purpose of a sinusoidal peak detector is to generate a DC output voltage which is proportional to the peak value of the input sinusoidal signal. Due to the waveforms of a power system, voltage and current are sinusoidal. A typical technique to design a peak detector employs op-amps as the active elements [3,20] along with filtering circuits. However, it may degrade the transient response of the sinusoidal peak detector. Hence, the transient performance of equipment that uses the typical technique can be improved by using the sinusoidal peak detector with fast transient response [21]. Therefore, the shortcomings are obviously a large configuration but a small operating frequency range and, not less important, a slow response due to the filtering.

In this paper, an electronically tunable peak detector comprising four CCCIIs, three MOS transistors, and a single grounded capacitor as a passive component is proposed aimed to get round the problems above. The angle pole frequency of the realized all-pass filter can be controlled electronically by means of bias current. The circuit provides operating frequency up to 20 MHz with increased linearity and precision in determining the peak value, and is suitable for integrated circuit implementation. Several time-domain and frequency-domain responses, total harmonic distortion (THD) and error analysis via HSPICE simulation program are given to verify the theoretical results.

The paper involves the following sections: Section 2 introduces new peak detector circuits, Section 3 addresses the non-ideality analysis for the proposed detector, while respective simulation results obtained using HSPICE program are evaluated in Section 4 which also provides the comparison of the proposed circuit and its parameters with other known realizations. The conclusions are considered in Section 5.

2. Proposed peak detector circuit

The proposed circuit of peak detector is shown in Fig. 1. The input sinusoidal signal can be represented as

$$v_{input}(t) = V_m \sin(2\pi f t) \tag{1}$$

where V_m is amplitude and f is frequency. The NMOS transistors (T_1, T_3) have positive threshold voltage V_{Tn}, while the PMOS transistor T_2 has negative V_{Tp}. The y ports of the first and second CCCIIs in Fig. 2 are biased at the threshold voltages of the MOS transistors as $V_{B1} = -V_{Tn}$ and $V_{B2} = -V_{Tp}$. The bulks of all of the PMOS transistors are connected to the source terminals, while the bulks of all of the NMOS transistors are connected to the V_{SS} (Fig. 2). The characteristics of the ideal CCCII are represented by

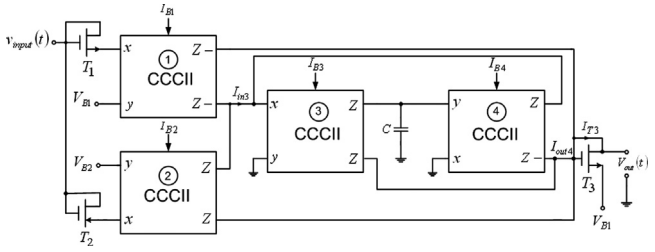

Fig. 1. The proposed circuit of the peak detector.

the following hybrid matrix:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{2}$$

If the CCCII is realized using CMOS technology, R_x can be respectively written as $R_x = \sqrt{1/(kI_B)}$, where k is the physical transconductance parameter of the MOS transistor defined as

$$k = 8\mu_p C_{oxp}(W_p/L_p)_{9-10} = 8\mu_n C_{oxn}(W_n/L_n)_{11-12} \tag{3}$$

I_B is the bias current used to control the intrinsic resistance at x port. In general, CCCII can contain an arbitrary number of z terminals, providing both directions of currents I_z. The internal construction of the CMOS CCCII is shown in Fig. 2. It should be noted that the first, second and third CCCII in Fig. 1 should have low impedance ($R_{x1,2,3} \cong 0$) by setting I_{B1}, I_{B2}, and I_{B3} at the highest possible value allowed by the proposed configuration of CCCIIs in order to achieve low input impedance of the filter and the first two CCCIIs. The real limit of the bias current is defined after simulation checks in Section 4. Also, the graph of the bias current versus R_x will be also included.

The phase shift (for 90°) of the square of the input signal is realized using an all-pass filter. The proposed current-mode first order all-pass filter is illustrated in Fig. 1. It consists of 2 CCCIIs and one grounded capacitor. Considering the circuit in Fig. 1 and using CCCII properties, the current transfer function can be rewritten as

$$\frac{I_{out4}}{I_{in3}} = \frac{sCR_{x4} - 1}{sCR_{x4} + 1} \tag{4}$$

The equation infers that the current gain of the proposed circuit is unity and has the phase response as

$$\angle H(\omega_p) = \phi(\omega_p) = 180 - 2\tan^{-1}(\omega_p C R_{x4}) \tag{5}$$

where $R_{x4} = \sqrt{1/k_4 I_{B4}}$. The Eq. (5) suggests that the circuit gives a phase shift from 0° TO (−180°). Moreover, the angle pole frequency can be electronically controlled by I_{B4}. The ω_p sensitivities of the filter can be rewritten as follows:

$$S_C^{\omega_p} = -1; \quad S_{I_{B4}}^{\omega_p} = S_{k_4}^{\omega_p} = 1/2 \tag{6}$$

Therefore, all of active and passive sensitivities are no more than unity in magnitude. If $v_{input}(t) > 0$, the current is conducted through the NMOS transistors T_1 to the output. However, if $v_{input}(t) < 0$, the PMOS transistor T_2 conducts the current to the output. Hence, the current–voltage relationships of the MOS transistors operating in saturation region can be respectively given by the square-law relation as

$$I_{T1} = \frac{k_n}{2}(v_{GS1} - V_{Tn})^2 = \frac{k_n}{2}v_{input}^2(t); \quad \text{for } v_{input}(t) > 0$$
$$I_{T2} = \frac{k_p}{2}v_{input}^2(t); \quad \text{for } v_{input}(t) < 0 \tag{7}$$

NMOS and PMOS transistors conduct in opposite halves of the input signal. Such control enables current input from the port z+ of the first CCCII on the all-pass filter at the interval in which the input voltage signal is positive, i.e. from the port z− of the second CCCII when the input voltage is negative. Assuming that

$$k_{n(T1-T3)} = k_{p(T2)} = k \tag{8}$$

for the proposed circuit it follows that

$$I_{T1} + I_{T2} + I_{out4} = \frac{k}{2}V_m^2 \sin^2(2\pi f t) + \frac{k}{2}V_m^2 \cos^2(2\pi f t) = \frac{k}{2}V_m^2 \tag{9}$$

The above represents the total current in the V_{out} node and it is equalised with the current of the T_3 transistor. It follows that

$$I_{T3} = \frac{k}{2}V_m^2 = \frac{k}{2}V_{out}^2(t) \tag{10}$$