Journal of Alloys and Compounds 731 (2018) 150–155

Contents lists available at ScienceDirect

Journal of Alloys and Compounds

journal homepage: http://www.elsevier.com/locate/jalcom

Solution-processed HfGdO gate dielectric thin films for CMOS application: Effect of annealing temperature

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A R T I C L E I N F O

Article history:
Received 8 August 2017
Received in revised form
22 September 2017
Accepted 3 October 2017
Available online 5 October 2017

Keywords:
Gate dielectrics
HfGdO thin films
Annealing temperature
X-ray photoelectron spectroscopy
Sol-gel

A B S T R A C T

Annealing temperature dependent microstructure, optical and electrical properties of sol-gel-deposited HfGdO high-k gate dielectric thin films on Si substrates are systematically investigated. X-ray spectroscopy (XPS) analyses have confirmed that the interfacial layer at HfGdO/Si interface is mainly silicate and the component increases with increasing the annealing temperature. Moreover, the band offsets for HfGdO/Si gate stack as a function of annealing temperature also have been determined. As a result, it can be noted that increase in valence band offset (ΔE_v) and reduction in conduction band offset (ΔE_c) have been detected. Electrical characterizations have indicated that higher annealing temperature effectively improves the electrical characteristics, such as the increased effective permittivity (k) and the decreased flat band voltage shift (ΔV_{fb}). However, due to the reduced ΔE_c and the appearance of crystallization, increased leakage current density has been observed with the increase in annealing temperature.

1. Introduction

In the previous decades, SiO_2 was chosen as the standard high-k gate dielectric material to be used in complementary metal oxide semiconductor (CMOS) devices due to its excellent compatibility with Si [1,2]. With the rapid development of ultra large scale integrated circuits, the conventional SiO_2-based gate dielectrics has reached its physical limit. Therefore, high dielectric constant (k) materials, such as Hf-based oxides and Zr-based oxides, are selected to resolve the large leakage current and high power consumption of SiO_2-based CMOS devices [3–6]. As an alternative candidate for high-k gate dielectric material, HfO_2 has moderate dielectric constant (~25), wide band gap (~5.6 eV), superior thermodynamic stability and appropriate band offset relative to Si substrate [7,8]. However, the lower crystallization temperature and high oxygen and impurities penetration prevent its application [9].

An effective method to overcome this issue is to incorporate another element into HfO_2 thin films. Based on some previous publications, it can be seen that HfO_2-based high-k gate dielectrics doped by rare earth oxides demonstrate increased dielectric constant, suppressed oxygen vacancies and improved electrical performance in CMOS devices application [10–15].

By far, various deposition methods have been adopted to obtain gate oxide thin films, such as sputtering, atomic layer deposition, sol-gel and so on. Among these methods, solution-based deposition method is gradually attracting more attention due to its simple operation, low cost and large-scale production [16]. By now, although several investigation about the evolution of the interface chemistry and electrical properties of Gd-doped HfO_2 high-k gate dielectrics have been investigated, there are few investigations on the preparation of Gd-doped HfO_2 thin film derived by sol-gel.

In current work, the rare earth (RE) Gd was selected to be incorporated into HfO_2 high-k gate dielectric thin films by using solution-based method. The effect of annealing temperature on the microstructure, band gap, interfacial and electrical properties of Gd-doped HfO_2(HfGdO) high-k gate dielectrics have been systematically investigated.

2. Experimental

HfGdO films were deposited on n-type Si substrates with a resistivity of 2–5 Ω cm. The precursor solution was prepared by dissolving metal salts in an appropriate solvent. In this work, gadolinium nitrate hexahydrate ($Gd(NO_3)_3 \cdot 6H_2O$, 99.9%) and hafnium chloride ($HfCl_4$, 99.9%) were chosen for the preparation of the precursor solution. The metal salts were dissolved in ethyl alcohol and the concentration of precursor solution was 0.1 M (the mole ratio of Hf:Gd was 2:1). The HfGdO thin films were deposited

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https://doi.org/10.1016/j.jallcom.2017.10.019
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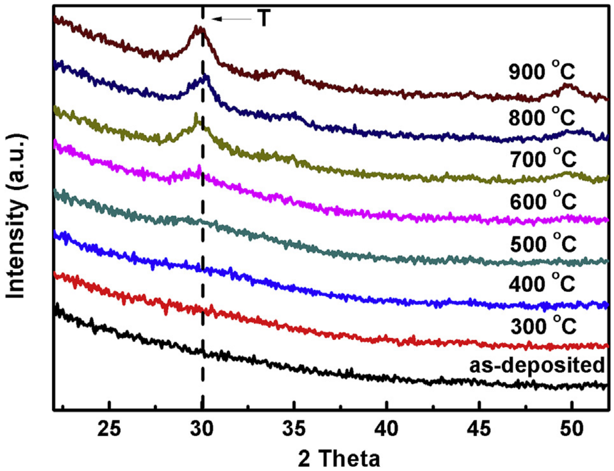

Fig. 1. XRD patterns of solution-derived HfGdO thin films annealed at different temperature.

by spin-coating at 5000 rpm for 30 s. Then a soft bake at 200 °C for 5 min was carried out to evaporate the organic solvent. After deposition, the samples were annealed in nitrogen ambient at 400 °C, 500 °C, 600 °C and 700 °C for 120 s. Based on the three-layer-structure (Si/SiO_2/HfGdO) and Cauchy-Urbach dispersion model, the thickness of HfGdO films was obtained by using spectroscopic ellipsometry (SE, SC630, SANCO Co, Shanghai). To investigate the evolution of the microstructure of HfGdO thin films as a function of annealing temperature, X-ray diffraction (XRD, MXP 18AHF MAC Science, Yokohama, Japan) measurements have been carried out. The interface chemistry of HfGdO/Si gate stacks were studied by X-ray photoelectron spectroscopy (XPS, ESCALAB 250Xi). To investigate the optical properties of HfGdO gate dielectrics by using a Ultraviolet–visible spectroscopy (UV–Vis, Shimadzu, UV-2550), HfGdO thin films were deposited on quartz wafers. The electrical properties of MOS capacitor based on HfGdO/Si gate dielectric were investigated by a semiconductor device analyzer (Agilent B1500A).

3. Results and discussion

Fig. 1 exhibits the XRD patterns of the as-prepared and annealed HfGdO gate dielectric thin films as a function of annealing temperature. Based on Fig. 1, it can be found that no apparent diffraction peaks have been detected for the as-deposited and annealed samples processed at 300, 400 and 500 °C, suggesting that the HfGdO films annealed at lower temperature still keep amorphous state. However, for the sample annealed at 600 °C, weak diffraction peak attributed to tetragonal phase of HfO_2 has been observed, which indicates that the crystallization for HfGdO thin films happens. With the increase in annealing temperature, the intensity of the diffraction peaks centered at 30° enhances and no other peaks have been detected, revealing that Gd incorporation into HfO_2 stabilizes tetragonal phase of HfO_2 regardless of annealing temperature.

Interface chemistry plays an important role in high-k/Si gate stack and the precise determination of the interfacial information will offer the criteria for choosing the suitable high-k gate dielectrics candidate for CMOS devices. By using XPS measurements, the evolution of the Hf 4f, Gd 3d, O 1s and Si 2p core-level spectra of HfGdO/Si gate stacks as a function of annealing temperature has been determined. By quantitative analysis, the chemical ratio of the HfGdO thin films annealed at 400, 500, 600 and 700 °C are calculated to be $HfGd_{0.581}O_{5.846}$, $HfGd_{0.748}O_{6.022}$, $HfGd_{0.790}O_{6.456}$ and $HfGd_{0.769}O_{7.046}$, respectively. The core level survey spectra obtained by XPS measurement have been demonstrated in Fig. 2. It can be found that except the peaks originating from Hf, Si, Gd, C, and O elements, there is no other peaks from other elements have been detected, indicating that the Gd has been incorporated in the HfO_2.

Fig. 3 displays the Hf 4f core-level spectra of HfGdO/Si gate stack as a function of annealing temperature. Based on some previous

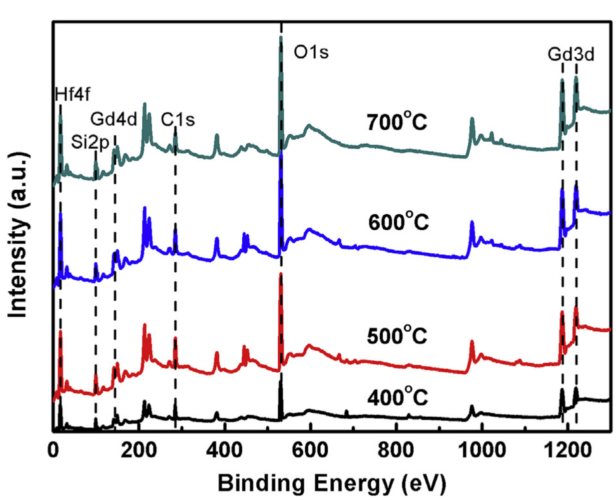

Fig. 2. The XPS survey spectra of HfGdO/Si gate stack annealed at 400, 500, 600 and 700 °C.

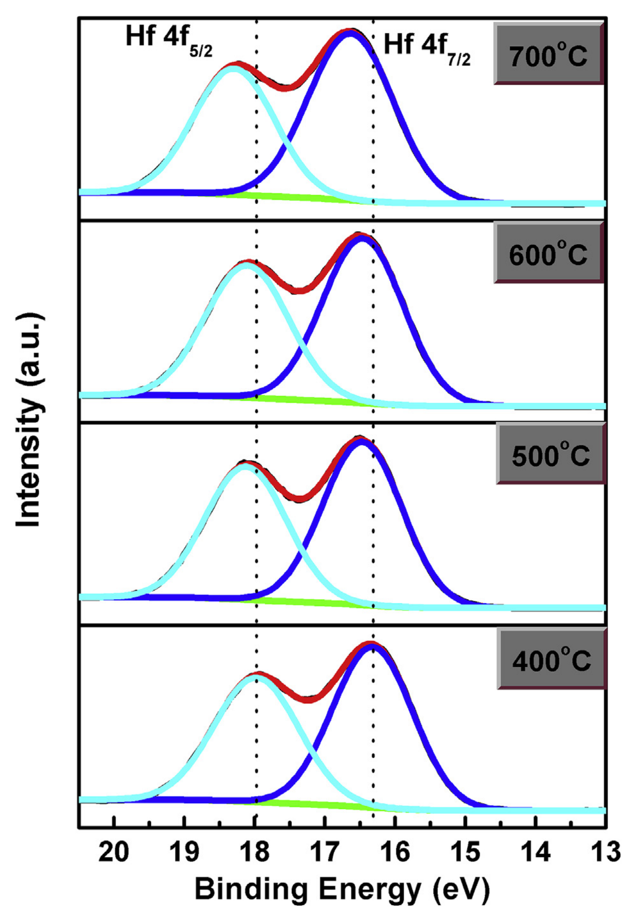

Fig. 3. Hf 4f XPS spectra of HfGdO/Si gate stack annealed at different temperature.