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p-NiO/n$^+$-Si single heterostructure for one diode-one resistor memory applications

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ABSTRACT

One diode-one resistor (1D1R) memory is one of effective architectures to suppress the crosstalk interference of crossbar network. The conventional 1D1R device usually consists of a stack of sandwich-structure memory and pn junction diode. Herein, we demonstrated a 1D1R device based on a single-stacked *p*-NiO/n$^+$-Si heterostructure, and its structure and fabrication process are greatly simplified compared with those of multilayer 1D1R devices. Studies on electrical transport properties reveal that the p-type NiO film not only serves as a resistive-switching layer, but also combines with n-type Si to form a pn heterojunction diode. Due to the existence of the built-in electric field, it can neutralize the applied external electric field and the nanoscale conducting filaments (CFs) are only confined to the outside of depletion region of NiO/Si pn junction. Thus, the formation of CFs does not degrade the diode quality, which allows the coexistence of resistive-switching and rectifying behaviors.

1. Introduction

Resistive random access memory (RRAM) has recently generated great interest as a leading candidate for next-generation nonvolatile storage technology. RRAMs offer some advantages over conventional charge storage memories, such as fast switching speed, high storage density, and low power consumption [1–3]. Great progress has been made both in improving the device performance and understanding the working mechanism [4,5], while research on device integration is proceeding at a rapid pace. A passive crossbar array is regarded as one of the most promising architectures for RRAM integration, due to the simplicity, scalability, and multiple stackability of this structure [6–8]. However, the crossbar array architecture suffers from an intrinsic crosstalk problem in practical applications. For a selected memory cell, the sneak path current through neighboring cells will lead to misreading operations and limit the number of integration cells. Recently, various nonlinear selectors, such as diode, transistor, complementary memristor has been made in the integration of 3D vertical RRAM to mitigate the crosstalk problem [9–13]. Among them, a diode in series with a RRAM, namely, 1D1R structure, is only compatible with the unipolar RRAM devices, and is also regarded as a cost-effective strategy due to the simple diode structure and easy fabrication process. For example, Seo et al. and Lee et al. have demonstrated 1D1R devices by introducing Pt/NiO/ZnO/Pt and Pt/CuO_x/$InZnO_x$/Pt heterojunction diodes, respectively, where the excellent rectifying characteristics could effectively eliminate the sneak paths [9,14]. Most of conventional 1D1R devices usually consist of a stack of sandwich-structure RRAM and pn junction diode, thus having a complex multilayer structure, which inevitably limits the complicates fabrication process.

In this work, we demonstrated 1D1R device based on a single-stacked heterostructure *p*-NiO/n$^+$-Si, and no interlayer, such as metal electrode, is inserted between the RRAM and diode components (Fig. 1(b)). Herein, the NiO film plays a dual role: the switching layer of RRAM device and the depletion layer of NiO/Si pn junction. The formation of nanoscale conducting filaments (CFs) in the NiO layer does not destroy the *p*-NiO/n$^+$-Si junction interface. Therefore, the stable resistive switching (RS) characteristics and high rectifying ratio both are achieved. The simple, single-stack 1D1R structure avoids the complex multilayer deposition process using different techniques. In addition, the use of Si material also facilitates the integration of metal oxide RRAMs with the mature Si-based microelectronic technology.

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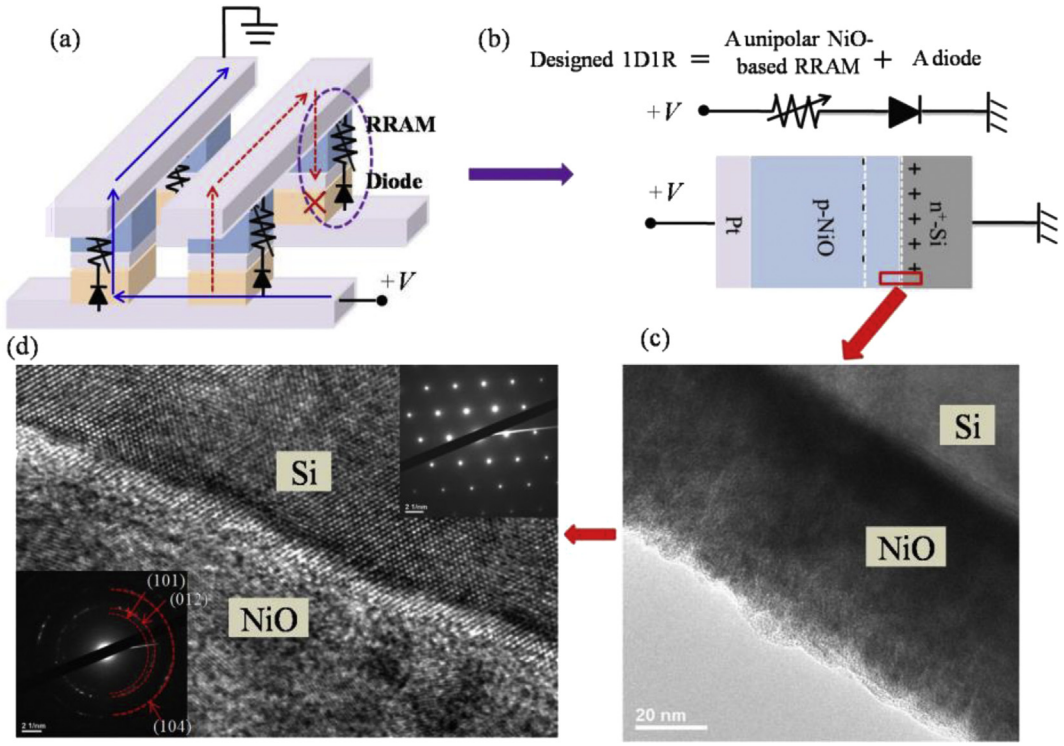

Fig. 1. (a) The typical 1D1R crossbar network (2 × 2). The blue solid line represents a read current through the selected memory cell, and the red dash line indicates a sneak path current through neighboring cells, which is blocked by the diode component of 1D1R structure. (b) A schematic diagram of the 1D1R device with a Pt/p-NiO/n^+-Si single-stacked structure. (c) and (d) The low-and high-resolution cross-sectional TEM images of NiO/Si heterostructure. The inset of Fig. 1(d) shows the selected area electron diffraction patterns of the Si and NiO films. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

2. Experimental conduction

A structural diagram of the Pt/p-NiO/n^+-Si 1D1R device is shown in Fig. 2(e). The heavily doped n-type Si substrate with a low resistivity of ~0.005 Ω cm was used to form the pn heterojunction. An Al metal film, as a bottom electrode, was deposited on the n^+-Si substrate to form an ohmic contact. Then, an about 60 nm-thick NiO film was grown on the n^+-Si substrate by magnetron

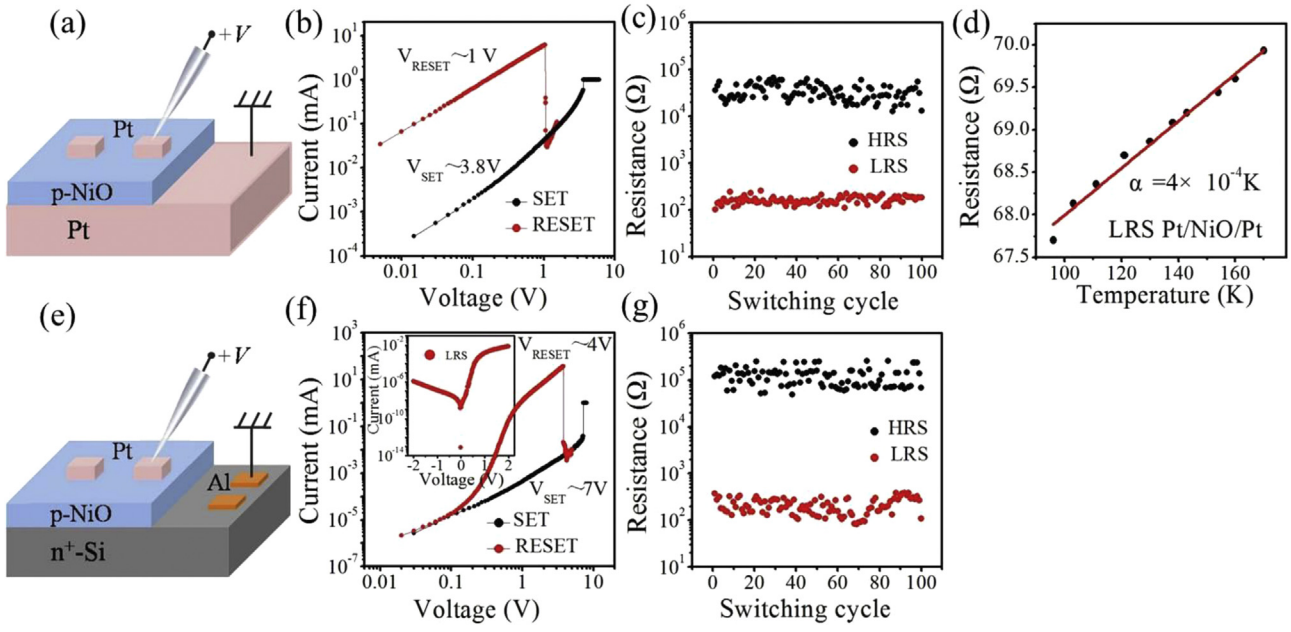

Fig. 2. (a) and (e) Structural diagrams of the reference device Pt/NiO/Pt and the 1D1R device Pt/p-NiO/n^+-Si. (b) and (f) The unipolar RS behavior of the reference device and the 1D1R device. The inset of (f) shows the LRS I–V curve of 1D1R device with a rectifying characteristic. (c) and (g) The HRS/LRS distributions of the two devices recorded in 100 continuous RS cycles. (d) The temperature dependence of LRS resistance of the reference device Pt/NiO/Pt, and the solid line is a linear fit to equation $R(T) = R_0 [1-\alpha(T-T_0)]$.